Curriculum Vitae – Michael J. Flynn

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Education and Professional Activities

Education:

B.S. Electrical Engineering, Manhattan College, New York, NY 1955
M.S. Electrical Engineering, Syracuse University, Syracuse, NY 1960
Ph.D. Electrical Engineering, Purdue University, West Lafayette, IN 1961
Sc. D. (*h. c.*) Computer Science, University of Dublin, Dublin, Ireland 1998

Engineering Licenses:

Professional Engineer (New York)
Chartered Engineer (Republic of Ireland)
EuroEngineer (European Federation of National Engineering Associations- FEANI)
Radio Licenses: U.S. Amateur (W2FRT) and experimental; Trustee (1985-2004) for Stanford radio club (W6YX), Ireland radio experimenter (EI9GW)

Current and recent Professional Activities:

Visiting Professor of Computer Science, Queen's University, Belfast, Northern Ireland (2002-2004)
Emeritus Professor of Electrical Engineering, Stanford University, Stanford, California, (1999--Present)
Director of the Stanford University Computer Architecture and Arithmetic Group (1992- Present)
Cheng Tsang Man Professor in Engineering, (Visiting Distinguished Professor) Nanyang Technological University (NTU), Singapore (2001)
Board of Advisors, Procket Networks, Freemont, California (2000-2004)
Board of Advisors, Arithmatica, Redwood City, California (2001- present)
Senior Planning Advisor and Director, Chalkboardnet, Inc. Milpidas, California. (2000-2003)
Senior Advisor, CTO and Director, CPO Technologies, Sunnyvale, California

Prior Professional Experience:

At Stanford University (1975--1999):
Professor of Electrical Engineering, Stanford University, Stanford, California (1975--1999)
Professor at Stanford Center for Technology and Innovation, Kyoto, Japan (1994 and 1996)
Director of the Stanford Emulation Laboratory (1976--1992)
Director of the Computer Systems Laboratory (1976--1983)
Director of the Stanford Computer Forum (1975--1988)
Director, Center for Aeronautics and Space Information Science, NASA-sponsored research center (1991--1995)

Other Activities while at Stanford:
1985--1994:
Chairman, Technical Advisory Committee, NCR Corporation
This was the primary external technical advisory committee to NCR management.

1984--1995:
General Partner, Paragon Venture Partners, Menlo Park CA
A fund for venture investment in emerging companies in information technology.

1983--85
American Supercomputers, Inc., Santa Clara CA (on leave from Stanford), Vice President for Engineering;
Directed a large-scale supercomputer effort.

1980--81
Visiting Professor of Computer Science, Trinity College, Dublin, Ireland (IDA Fellowship, Sabbatical)

1973--1999:
Palyn Gould Group, Campbell, California, Senior consultant (1975--1999)
Co-founder and Vice President (1972--74) ---Consultant to many of the major computer manufacturers throughout the world.

Designer of `EMMY' computer---a research computer for emulation and interpretive computing (extension and implementation of a ``dynamic microprogrammed processor''---see publications). The EMMY design was licensed by ICL (UK) and produced as the ME-29. This was one of the most widely sold general-purpose computers in Europe during the early 1980's.

1970--1975
The Johns Hopkins University, Baltimore, Maryland, Professor of Computer Science/ Electrical Engineering

1966--1970
Northwestern University, Evanston, Illinois, Associate Professor in the Departments of Electrical Engineering and Industrial Engineering and Management Sciences.

1965--1966
University of Illinois at Chicago, Associate Professor, Systems Engineering

1955 –1970
IBM Corporation, consultant (1965- 1970)
IBM Corporation, Poughkeepsie, New York (1961- 1965)
Advisory Engineer responsible for planning (particularly memory) of IBM System/360
Manager, prototype development of IBM 7094 II
Manager, responsible for design and development of IBM System/360 Model 91/92/95 series CPU. The Model 90 series has been IBM's largest and highest performance computer system.

1959--1961
Purdue University, Visiting Instructor of Electrical Engineering (IBM fellowship)

1955--1959
IBM Corporation, Endicott and Poughkeepsie, New York
Design engineer in circuit and device design
Technical Consultant to IBM World Trade Corp., Paris (1956--57)
Manager, prototype development of IBM 7090 (1958--59)
Manager, Circuit Development Group, high-speed switching circuit development (1959)

Awards

Awards

- 2004 Outstanding Achievement Award, the World Academy of Science,

  "In recognition and appreciation of his dedicated and outstanding contributions to the field of Computer Architecture"
  2004 International Multi conference in Computer Science and Computer Engineering, Las Vegas NV, 21 June 2004

- Fellow, World Innovation Foundation, 24 November 2003
- Arith15 Dedication award, the 15th International Symposium on Computer Arithmetic was dedicated

  "to Michael J Flynn for his lasting contributions to the field"
  ARITH 15, Santiago de Compostela, Spain 15-18 June 2003

- The Tesla Award and Medal, from the International Tesla Society (Belgrade), August 1998.

  "For important contributions to computer architecture"

- Doctor of Science degree *honoris causa* from Trinity College (University of Dublin), Ireland. July 1998.
- IEEE Computer Society Golden Core Award (1996)
- 1995 IEEE Computer Society Harry Goode Memorial Award and Medal in recognition of an outstanding contribution to the information processing field.

  ``For pivotal seminal contributions to the design and classification of computer architecture."

- 1992 ACM/IEEE Eckert--Mauchly Award
  For technical contributions to computer and digital systems architecture.

  ``For important and seminal contributions to processor organization and classification, computer arithmetic and performance evaluation."

- Fellow, the Association for Computing Machinery (1994) "For outstanding contributions to the computer field"
- EuroEngineer, Federation of European Engineering Associations, 1989
- Fellow, the Institution of Engineers of Ireland (1981) "For service to the profession"
- IDA Fellow, 1980-1981
- Fellow, the Institute of Electrical and Electronic Engineers (1980) "For outstanding contributions to the field of computer architecture"
- IEEE Computer Society Honor Roll, 1977
- ACM Service Award, 1975

Honorary Societies:

Eta Kappa Nu (The Electrical Engineering honor society)
Sigma Xi (The Engineering honor society)
Tau Beta Pi (The Research honor society)

Research

Current Research:

Microprocessor architecture and VLSI support tools.
Computer Architecture and Organization
Parallel Processors and Processes
Computer Arithmetic
Optical Interconnections
Neural Basis for Computing

Recent Research Contracts:

Stanford University-Tohoku University Joint Research Program on Computer Architecture (1985- present)

"Tools for Computer Architecture" Ogawa Foundation Grant, Tokyo (2000-2001)

"ADAPTIVE Arithmetic", Alteria Corporation, Campbell CA (1999-2000)

"New Strategies and Architectures for Brain Imaging: the confluence of Genetic Probes, Micro- MRI and Multi- Modal Informatrics," DARPA/ ITO (1998-2001)

"Sub-Nanosecond Arithmetic", National Science Foundation, MIP 88-22961 (1988-1992) and (1993-1996)

Smart Photonic Networks and Computer Security for Image Data, Focused Research Initiative, BMDO (Army Research Office) 1995-1998

"Re-configurable Multimode, Multi-band Information Transfer System", Adaptive Computing Systems Program, DARPA, Department of the Army, (1997-2000)

"Design of Testbed and Emulation Tools", NASA Grant NAG 2-248, NASA Ames Research Center (1988-1996)

"Center for Aerospace Information Science, CASIS" NASA Interdisciplinary Research Center, (1980-1994)

"Visualization of Distributed System Performance", Digital Equipment Corporation, Maynard, MA, (1990-1992)

``Studies in Computer Concurrency and Sparse Memory," NASA RIACS, (1990-1992)

``Architecture Evaluation: Tools for the Software Technology Acceleration Project," Institute for Defense Analysis

``Concurrent System Performance Projection," NASA

``Studies in Advanced Architecture for Knowledge-Based Systems," NASA CESDIS

"Studies in Computer Organization", AEC and ERDA and Department of Energy, (1969- 1986)

Professional Service Activities

External University Service (recent only)

Member, Industrial Advisory Board, Computer Engineering Program, California Polytechnic University, San Luis Obispo, CA (2002- present)
Advisor, Entrepreneurship program, Harvey Mudd College, Pomona, CA (2001-2002)
External Examiner, Graduate School of Information Science, Tohoku University, Sendai, Japan (2000)
External Examiner, Electrical Engineering Department, Princeton University, Princeton, N. J.
External Examiner, Computer Engineering Department, University of Hong Kong (1998-2000)

Government Service

Member, Science Council for Universities Space Research Association (NASA).
Institute for Computer Applications in Science and Engineering (NASA), 1982--89.
Member, U. S. Air Force Science Advisory Board, 1973.
Member, Scientific and Management Advisory Committee to the Army Computer Systems Command, 1971--1974.
Member, Advisory Committee to the SAFEGUARD System Evaluation Agency (Dept. of the Army), 1970--1972.
Chairman, National Academy of Sciences/National Research Council Advisory Committee on Data Processing for Anti-Ballistic Missile Defense (1969--1972)
Consultant to the Department of Defense (Army Research Office) (1968--1972)
Consultant to the Applied Math Division, Argonne National Lab., Argonne, IL (1965--1973)

Professional Society Service:

Member IEEE Awards Committee (1991--1994)
Member IEEE Fellows Committee (1980--1985)
Vice President, IEEE Computer Society (1973--1975)
Member, Board of Governors, IEEE Computer Society (1970--75 and 1993--95)
Founding Chairman, Assoc. for Computing Machinery (ACM) Special Interest Group on Computer Architecture (SIGARCH) (1971--1973)
Founding Chairman, IEEE Technical Committee on Computer Architecture (1970--1973)
Member, Research Committee, Instrumentation Society of America (1968--1971)
Vice Chairman, IEEE Computer Society Chicago Chapter (1967--1968)

Professional Publication Service:

Advisory Board, IEEE Micro Journal (2004- present)
Editorial Board, IPSI Journal on Systems (2004- present)
Editorial Board, The Computer Journal (London) (2003- present)
Editorial Board, Journal of Parallel and Distributed Computing (Area editor for ``Advances in Computer Technology." (1984--2003)
Editorial Board, Information Sciences (1990--2004)
Editorial Board, Proceedings of the IEEE (1971--1974)
Associate Editor, Computer Architecture and Systems, IEEE Transactions on Computers (1971--1973)

Major Conference Service:

Program Chair, Hot Chips Conference 2003, Stanford CA, 17-19 August 2003
Chairman, Advisory Committee for the COOL Chips conference series (1997- present)
Conference Chairman, ARITH13 (13th Symposium on Computer Arithmetic), Asilomar, Pacific Grove, California, 7-9 July 1997
Conference Chairman, HPCA3 (3rd Symposium on High-Performance Computer Architecture), San Antonio, Texas, 3-5 February 1997
Conference Chairman, ISCA3 (3rd International Symposium of Computer Architecture), Florida, January 1976
Conference Chairman, MICRO3 (3rd Symposium on Micro-architecture/Microprogramming), Buffalo, New York, 1970
Member, Board of Trustees, National Electronics Conference, Inc. (1966--1969)

Lectureships (Summary—see last section for more complete list):

Keynote Lecturer: IPSI (Interdisciplinary conference on Internet, Processing and Systems) 2004, Pescara, Italy, July 2004
Keynote Lecturer: 2004 International Multi conference on Computer Science & Engineering, Las Vegas, NV, June 2004
Keynote Lecturer: SBAC (Brazilian Symposium on Computer Architecture), Sao Paulo, Brazil, November 2003
Plenary Lecturer: ACM Federated Computer Science Conferences, San Diego, June 2003
Distinguished Lecturer, University of Texas, Austin TX, March 2003
Keynote Lecturer: ICFPL, Hong Kong, December 2002
Distinguished Lecturer, Southern Methodist University, Dallas, TX, November 2002
Cheng Tsang Man Distinguished lectures (3), Nanyang Technological University, Singapore, October 2001
Keynote Lecturer: FPT, Belfast NI, August 2001
Keynote Lecturer: ACSAC 2001, (Australian Computer Science Week) Bond University, Gold Coast, January 2001;
Keynote Lecturer: Tohoku GSIS Anniversary Symposium, Sendai, Japan, November 2000;
Keynote Lecturer: COOL Chips II, Kyoto, Japan, May 1999.
Keynote lecture, MICRO30, Durham, North Carolina, 2 December 1997
Keynote Lecturer: ARCS (Architekur von Rechensystemen) Rostock, Germany, September 1997
Keynote Lecturer: EuroMicro, Budapest, Hungary, September 1997
Distinguished Lecturer, University of Texas, September 1996
Distinguished Lecturer, , University of Tromso, Norway, September 1996
Distinguished Lecturer, USC, April 1996
Distinguished Lecturer, Southern Methodist University, Dallas, Texas, April 1993
Distinguished Lecturer, EPLI--Lausanne, Switzerland, October 1991
Distinguished Lecturer, Georgia Tech, May 1991
Distinguished Lecturer, UCLA, March 1991
Keynote lecture, MICRO23, Orlando, Florida, November 1990
Summer lecturer, Jaio Tung University, Shanghai, China, 1986.
Keynote lecture, MICRO16, Downingtown, Pennsylvania, October 1983
Keynote lecture, MICRO15, Palo Alto, California, October 1982
Summer lecturer and Director; Advanced Course on Microcomputer System Design, Trinity College, Dublin, Ireland, June 1981.
Summer lecturer; Advanced Operating Systems, Institut Fur Informatik, Technical University Munich,1977
Distinguished Lecturer, IEEE Computer Society, 1972--1973.
Summer lecturer; in Microprogramming, University of Pennsylvania, 1972.
Summer lecturer; Institute de Recherche d'Info. et d'Autom. Paris, 1971.
Summer lecturer; NATO Workshop on Microprogramming, St. Raphel, France, 1971.
ACM (Assoc. for Computing Machinery) National Lecturer, 1969--1972.

Books and Patents

Books

Shlomo Waser and Michael J. Flynn.
Introduction to Arithmetic for Digital Systems Designers.
Holt, Rinehart, and Winston, New York, 1982, 302 pages.

M. J. Flynn, N. R. Harris, and D. P. McCarthy, Editors.
Microcomputer System Design: Lecture Notes in Computer Science.
Dublin, 1981, Springer-Verlag, 1984, 397 pages.

Jerome C. Huck and Michael J. Flynn.
Analyzing Computer Architectures.
IEEE Computer Society Press, New York, 1989, 208 pages.

Michael J. Flynn.
Computer Architecture: Pipelined and Parallel Processor Design.
Jones and Bartlett, Boston, 1995, 788 pages.

Michael J. Flynn and Stuart Oberman.
Advanced Computer Arithmetic Design.
John Wiley and Sons, New York, 2001, 325 pages

Patents:

"Execution Unit Shared by Plurality of Arrays of Virtual Processors."
U.S. Patent 3,611,307, October 5, 1971.

``Apparatus and Method in a Multiple Operand Stream Computing System for Identifying the Specification of Multi-Task Situations and Controlling the Execution of Said Tasks." U.S. Patent 3,614,745, October 19, 1971.

Theses:

M. J. Flynn.
Change Control Equivalent Circuit for Amplifiers.
MS Thesis, E.E.Department, Syracuse University, June 1960.

M. J. Flynn.
Operations in an Associative Memory.
Ph.D. Thesis, Purdue University, BTP-62-1782, APFILS, June 1961.

Publications I: Journal Papers and Refereed Conference Papers

M. J. Flynn and G. D. Bruce.
``Complementary Transistor-Resistor Logic,"
AIEE Winter General Meeting Preprints, January 1959.

M. J. Flynn and D. S. Henderson.
``Variable Field-Length Data Manipulation in a Fixed Word-Length Memory,"
IEEE Transactions on Electronic Computer, EC-12(5):512--517, October 1963.

M. J. Flynn and G. M. Amdahl.
``Engineering Aspects of Large High-Speed Computer Design,"
Proceedings of the Symposium on Microelectronics and Large Systems, (Office of Naval Research).

Revised version of above published as
``Large, High Speed Computer Design" chapter in Microelectronics and Large Systems.
Ed. Mathis, Wiley and Spandorfer. Spartan Books and Macmillan, Ltd., 1965.

M. J. Flynn.
``Complex Integrated Circuit Arrays: The Promise and the Problems."
Electronics, 39:11--116, July 1966. 7/11/66

M. J. Flynn.
``A Prospectus in Integrated Electronics and Computer Architecture,"
AFIPS Conference Proceedings, 29:97--103, Fall Joint Computer Conference, San Francisco, CA, November 1966.

M. J. Flynn.
``Very High-Speed Computing Systems,"
Proceedings of the IEEE, 54(12):1901--1909, December 1966.

M. J. Flynn and P. R. Low.
``The IBM System 360 Model 91: Some Remarks on System Development,"
IBM Journal of Research and Development, 11(1):2--7, January 1967.

R. A. Aschenbrenner, M. J. Flynn, and G. A. Robinson.
``Intrinsic Multiprocessing,"
AFIPS Conference Proceedings, 30:81--86, Thompson Book Company, Washington, D.C., Spring Joint Computer Conference, Atlantic City, NJ, April 1967.

M. J. Flynn and D. MacLaren.
``Microprogramming Revisited."
Proceedings of the Association of Computing Machinery Conference, 22:457--464, Thompson Book Company, Washington, D.C., 1967.

M. J. Flynn.
``Complex Arrays" (a version of the preceding article), Chapter 3 in Integrated Circuits and Packaging, Ed. G. Sideras, McGraw-Hill, 1968.

M. J. Flynn.
``The Use of a Technology: Function vs. Memory in LSI,"
Proceedings of the Second IEEE Computer Group Conference, Los Angeles, CA, June 1968.

S. S. Sisson and M. J. Flynn.
``Addressing Patterns and Memory Handling Algorithms,"
Fall Joint Computer Conference, San Francisco, CA. AFIPS Conference Proceedings, 33(II):957--967, December 1968. (Part II)

M. J. Flynn, A. Podvin, and K. Shimizu.
``A Multiple Instruction Stream Processor with Shared Resources,"
presented at ONR Symposium on Parallel Processors, Monterey, CA, June 1969

Above also appears in Parallel Processor Systems Technology and Applications,
Ed. L. C. Hobbs, et al., Spartan Books, 1970.

M. J. Flynn.
"Organization of Computing Systems", (2 chapters)
Computer and Program Organization, University of Michigan Engineering Summer Conferences, Ann Arbor, 1969.

M. J. Flynn and W. Snow.
``Multi-planer Self-Restricting Mazes: Some Results and Systems Applications,"
Proceedings of the Third Hawaii International Conference on System Sciences, Honolulu, January, 1970.

R. W. Cook and M. J. Flynn.
``System Design of a Dynamic Microprocessor,"
IEEE Transactions on Computers, C-19(3):213--222, March 1970.

M. J. Flynn.
``On Division by Functional Iteration,"
IEEE Transactions on Computers, C-19(8):702--706, August 1970.
Also appears in ***Benchmark papers in Electrical Engineering and Computer Science, pub IEEE, 1979***

G. S. Tjaden and M. J. Flynn.
``Detection and Simultaneous Execution of Independent Instructions,"
IEEE Transactions on Computers, C-19(10):889--895, October 1970.

S. Szygenda and M. J. Flynn.
``Coding Techniques for Failure Recovery in a Distributive Modular Memory Organization,"
American Federation of Information Processing Societies (AFIPS) Conference Proceedings, (SJCC) 38:459--566, 1971.

S. Szygenda and M. J. Flynn.
``Failure Analysis of a Memory Organization for Utilization in a Self-Repair Memory System,"
IEEE Transactions on Reliability, R-20(2):64--70, May 1971.

M. J. Flynn.
``Microprogramming: Future Prospects and Trends,"
IEEE International Convention Record, 1971, pp. 318--319.

A. B. Tucker and M. J. Flynn.
``Dynamic Microprogramming: Processor Organization and Programming,"
Communications of the ACM, 14(4):240--250, April 1971.

M. J. Flynn and R. F. Rosin.
``Microprogramming: An Introduction and a Viewpoint,"
IEEE Transactions on Computers} C-20(7):721--731,
July 1971 (A guest editor of this special issue on Microprogramming.)

M. J. Flynn.
``Shared Internal Resources in a Multiprocessor,"
(presented at IFIP Congress, Ljubljana, Yugoslavia).
In Information Processing 1971, pp. 565--569, N. Holland Pub. Co. 1972.

M. J. Flynn and S. Szygenda.
``A Perspective on Computer Reliability,"
In Proceedings of 1972 Symposium of Reliability and Maintainability, San Francisco, CA, January 1972.

M. J. Flynn.
``Multiprocessors with Shared Resources,"
IEEE International Convention Record, pp. 356--357, New York, March 1972.

M. J. Flynn and A. Podvin.
``An Unconventional Computer Architecture: Shared Resource Multiprocessing,"
IEEE Computer, 5(2):20--29, March / April 1972.

M. J. Flynn.
``Toward more efficient computer organizations,"
presented at the Spring Joint Computer Conference, Atlantic City, N.J.
In American Federation of Information Processing Societies (AFIPS) Conference Proceedings, 40:1211--1217, May 1972.

T. G. Hallin and M. J. Flynn.
``Pipelining of Arithmetic Functions,"
presented at IEEE Computer Society's Workshop on Computer Arithmetic, May 1972, College Park, MD.
In IEEE Transactions on Computers, C-21(8):880--886, August 1972.

T. G. Hallin and M. Flynn.
``Pipelining of Arithmetic Functions,"
(a version of the preceding paper). In COMPCON Proceedings, San Francisco, CA, September 1972.

M. J. Flynn.
``Some Computer Organizations and Their Effectiveness,"
IEEE Transactions on Computers, C-21(9):948--960, September 1972.

The above also appears in 1973 ***Best Computer Papers,*** pp.121--146,
Ed. I. L. Auerbach, Auerbach Pub., Philadelphia, PA., 1973.
This paper was one of two selected as the ***best papers submitted to the IEEE Transactions on Computers during 1972.***

S. Szygenda and M. Flynn.
``Self-Diagnosis and Self-Repair in Memory: An Integrated System Approach,"
IEEE Transactions on Reliability, R-22(2), April 1973.

M. J. Flynn.
``Computer Architecture at Johns Hopkins."
Computer Architecture News, (pub ACM-SIGARCH}) 1(2):21--33, April 1972.

M. J. Flynn.
``Open Problems in Microprogamming,"
Proceedings (Supplement) of the Sixth Hawaii International Conference on Systems Sciences, Honolulu, January 1973.

G. S. Tjaden and M. J. Flynn.
``Representation of Concurrency with Ordering Matrices,"
IEEE Transactions on Computers, C-22(8):752--761, August 1973.

R. W. Cook and M. J. Flynn.
``Logical Network Cost and Entropy,"
IEEE Transactions on Computers} C-22(9):823--826, September 1973.

M. J. Flynn.
``Open Problems in Microprogramming," (identical to the above paper)
INFOTECH State of the Art Report 17: Computer Design, Pub. INFOTECH Info. Tech Ltd., 1974.

M. J. Flynn.
``Computer Organizations and their Uses,"
Proceedings of the Third Texas Conference on Computing Systems, November 1974.

M. J. Flynn.
``Microprogramming"
and a number of shorter articles in Encyclopedia of Computer Science, (A. Ralston, Ed.), Auerbach, 1975.

M. J. Flynn.
``Microprogramming Concepts,"
Software Systems Principles, (P. Freeman, Ed.).
Science Research Associates, 1975.

M. J. Flynn.
``Trends and Problems in Computer Organization" (invited paper),
IFIP Congress '74, pp. 2--10, Stockholm, Sweden, August 1974; North Holland Pub. 1975.

M. J.Flynn.
`` Microprogramming'---Another Look at Internal Computer Control"
(invited paper), Proceedings of the IEEE, 63(11), November 1975.

M. J. Flynn.
``Interpretation, Microprogramming and the Control of a Computer" (similar to above paper).
Chapter 10 in Introduction to Computer Architecture, Ed. H. Stone, pp. 432--473. Science Research Associates, 1975.

M. J. Flynn, C. Neuhauser, and R. M. McClure.
``EMMY: An Emulation System for User Microprogramming,"
National Computer Conference, Anaheim, CA. In AFIPS Conference Proceedings, 44:85--89, May 1975.

R. M. McClure and M. J. Flynn.
``An Integrated Facility for Emulation Research,'
In 2nd USA--Japan Computer Conference Proceedings, pp. 42--47, Pub. AFIPS, August 1975.

M. J. Flynn and R. Kosaraju.
``Processes and Their Interactions,"
Special Issue of Kybepnhthe, 5:159--163, 1976.

M. J. Flynn.
``Non-Specific Computers,"
In COMPCON Proceedings pp. 3--5, February 1976.

M. J. Flynn.
``Some Remarks on High Speed Computers,"
IEEE Spring COMPCON Digest of Papers, pp. 18--20, February 1977.

M. J. Flynn.
``The Interpretive Interface: Resources and Program Representation in Computer Organization,"
Proceedings of the Symposium on High Speed Computers and Algorithm Organization, pp. 41--69, Pub. Academic Press, University of Illinois, Champaign, IL, April 13--15, 1977.

M. J. Flynn.
``Computer Organization and Architecture,"
Lecture Notes on Advanced Operating Systems, pp. 17--98, Pub. Springer-Verlag, 1978.

Philip S. Yu and M. J. Flynn.
``Performance Analysis of Distributed Computer Systems,"
Proceedings of the Sixth Texas Conference on Computer Systems}, Austin, Texas, November 1977.

M. J. Flynn.
``Non-Specific Computers" (invited paper).
INFOTECH Future Systems Report, pp. 153--168, 1977.

M. J. Flynn.
``Classes of Emulators,"
SIGMICRO Newsletter, 8(4):34--35, December 1977.

M. J. Flynn.
``VLSI: The Next Computer Generation,"
The Stanford Engineer pp. 19--24, Fall/Winter 1979.

M. J. Flynn and J. L. Hennessy.
``Parallelism and Representation Problems in Distributed Systems,"
Proceedings of the 1st International Conference on Distributed Computing Systems, pp. 124--130, Huntsville, AL, October 1979.

M. J. Flynn.
``Division by Functional Iteration" (a reprint of an earlier paper),
in Computer Arithmetic, Vol. 21 in Benchmark papers in Electrical Engineering and Computer Science Series. Ed. E. Swartzlander, Jr., Pub. Academic Press, November 1979.

M. J. Flynn.
``Interpretation, Microprogramming and the Control of a Computer,"
Chapter 10 of Introduction to Computer Architecture, 2nd Edition. Ed. H. Stone, Science Research Associates, Pub. 1980.

M. J. Flynn.
``Directions and Issues in Architecture and Language,"
Computer, 13(10):5--22, October 1980.

M. J. Flynn and J. L. Hennessy.
``Parallelism and Representation Problems in Distributed Systems,"
IEEE Transactions on Computers, C-29(12):1080--1086, December 1980.

M. J. Flynn.
``Perspective on Microcomputers," in Microcomputer System Design.
Edited by M. J. Flynn, N. R. Harris and D. P. McCarthy.
Lecture Notes in Computer Science, Dublin 1981, Pub. Springer-Verlag, pp. 1--8.

M. J. Flynn.
``Customized Microcomputers" in Microcomputer System Design.
Edited by M. J. Flynn, N. R. Harris and D. P. McCarthy,
Lecture Notes in Computer Science, Dublin 1981. Pub. Springer-Verlag, pp. 182--222.

M. J. Flynn and J. C. Huck.
``Analysis of Architectures for High Level Languages," a collection of papers in the
Workshop on High-Level Language Computer Architecture, Los Angeles, CA, October 1981, pp. 5-1--5-24.

R. Wedig and M. J. Flynn.
``Concurrency Detection in Language-Oriented Processing Systems," Third International Conference on Distributed Computing Systems, Miami/Ft. Lauderdale, FL, October 1982.

M. J. Flynn, J. C. Huck, S. P. Wakefield and R. Wedig.
``Performance Evaluation of the Execution Aspects of Computer Architectures,"
International Workshop on High-Level Language Computer Architecture, Ft. Lauderdale, FL, December 1982.

M. J. Flynn and L. W. Hoevel.
``Execution Architecture: the DELtran Experiment"
IEEE Transactions on Computers, C-32(2):156--174, February 1983.

J. C. Huck and M. J. Flynn.
``Comparative Analysis of Computer Architectures,"
Proceedings of IFIP Congress '83, Paris, September 1983.

M. J. Flynn.
``Stanford Emulation Laboratory,"
ACM SIGMicro Newsletter 14(3):10--17, September 1983.

M. J. Flynn.
``Towards Better Instruction Sets,"
Proceedings, 16th Annual Microprogramming Workshop, ACM SIGMicro Newsletter 14(4): 3--8, October 1983.

D. Alpert, M. Flynn, and S. Wakefield.
``Directly Executed Language Architectures for VLSI Processor Design,"
Proceedings of IEEE International Conference on Computer Design, pp. 609--612, New York, NY, October 1983.

M. J. Flynn, N. R. Harris and D. P. McCarthy, Eds.
Customized Microcomputers chapter in Microcomputer System Design---An Advanced Course.
Springer Study Edition, pp. 182--222, Springer-Verlag 1984.

M. J. Flynn and J. C. Huck.
`Emulation' chapter in Handbook of Software Engineering, pages 134--148.
Edited by C. R. Vick and C. V. Ramamoorthy.
Van Nostrand Reinhold Co., 1984.

M. J. Flynn and L. Hoevel,
``Measures of Ideal Execution Architectures,"
IBM Journal of Research and Development, 28(4):356-369, July 1984

M. J. Flynn, J. D. Johnson, and S. P. Wakefield.
``On Instruction Sets and Their Formats,"
IEEE Transactions on Computers, C-34(3):242-254, March 1985.

M. J. Flynn, C. Spangler, and A. Zimmerman.
``The Stanford Packet Radio Network," IEEE Computer Society
COMPCON Spring '86 Digest of Papers. pp. 266--268

T-F. Ngai, J. Yan, V. Mak, S. Lundstrom, and M. Flynn.
``Mapping between Parallel Processor Structures and Programs,"
Proceedings of the 20th Hawaii International Conference on Systems Sciences, January 1987.

B. P. Boesch and M. .J. Flynn.
``Effects of Layered Protocols on Performance of a Packet Radio Network,"
Proceedings COMPCON Spring '87.

S. P. Wakefield and M. J. Flynn.
``Reducing Execution Parameters through Correspondence in Computer Architecture,"
IBM Journal of Research and Development, 31(4):420--434, July 1987.

M. J. Flynn, C. L. Mitchell, and J. M. Mulder.
``And Now a Case for More Complex Instruction Sets,"
IEEE Computer. 20(9):71--83, September 1987.

C. L. Mitchell and M. J. Flynn,
``A Workbench for Computer Architects,"
IEEE Design & Test, 5(1):19--29, February 1988.

D. Alpert and M. J. Flynn.
``Performance Tradeoffs for Microprocessor Cache Memories,"
IEEE Micro} 8(4):44--54, August 1988.

G. Bewick, P. Song, G. DeMicheli and M. Flynn.
``Approaching a Nanosecond: A 32-bit Adder,"
in Proceedings, International Conference on Computer Design, October 1988.

M. J. Flynn,
Foreword to High-Level Language Computer Architecture,
V. M. Milutinovic, editor. Computer Science Press, New York, NY, 1989.

M. J. Flynn and R. I. Winner.
``ASIC Microprocessors,"
Proceedings, 22nd International Workshop on Microprogramming, Dublin, August 1989.

D. Wong, G. De Micheli, and M. Flynn.
``Designing High-Performance Digital Circuits Using Wave Pipelining,"
Proceedings, IFIP Conference on VLSI, Munich, August 1989.

B. Bray, K. Cuderman, M. Flynn, and A. Zimmerman.
``The Computer Architect's Workbench,"
In Information Processing 89, pages 509--514, September 1989.
Elsevier Science Publishers B.V. (North-Holland).

D. Wong, G. De Micheli, and M. Flynn.
``Inserting Active Delay Elements to Achieve Wave Pipelining."
In Proceedings of ICCAD '89, pp. 270--273, Santa Clara, CA, November 1989.

K. Nowka and M. J. Flynn,
``The Pipelined Processor as an Alternative to VLIW,"
In Proceedings of the Third International Supercomputing Conference, Santa Clara, CA, 1989.

T. M. Pinkston and M. J. Flynn.
``Parallel Processor Memory Reference Analysis and its Application to Interconnect Architecture,"
In Proceedings of the 5th Distributed Memory Computing Conference, Charleston, SC, pages 697--702, April 1990.

C. Mitchell and M. Flynn.
``The Effects of Processor Architecture on Memory Traffic,"
Transactions on Computer Systems, 8(3):230--250, August 1990.

P. K. Dubey and M. J. Flynn.
``Optimal Pipelining,"
Journal of Parallel and Distributed Computing, Volume 8, pages 10--19, 1990.

M. J. Flynn
``Instruction Sets and Their Implementations."
IEEE/ACM Proceedings of Micro-23, Orlando, FL, Keynote speech.
C. Papachristou, ed, pages 1--6, November 1990.

J. M. Mulder, N. T. Quach, and M. J. Flynn.
``An Area Model for On-Chip Memories and Its Application,"
Journal of Solid State Circuits. February 1991.

F. F. Lee, M. J. Flynn, and M. Morf.
``Design of Compact High Performance Processing Elements for the FCHC Lattice Gas Models,"
Proc. 5th SIAM Conf. on Parallel Processing for Scientific Computing, March 1991.

D. Wong and M. J. Flynn.
"Fast division using accurate quotient approximations to reduce the number of iterations".
Proceedings of the 10th Symposium on Computer Arithmetic, Grenoble, France, June 1991.

F.F. Lee and M.J. Flynn.
"Architectural Mechanisms to Support Three-Dimensional Lattice Gas Simulations".
Proceedings of the Third Annual ACM Symposium on Parallel Algorithms and Architectures, pages 115--122, July 1991.

E. M. Schwarz and M. J. Flynn.
``Cost-efficient high-radix division,"
Journal of VLSI Signal Processing 3(4): 293-305. (Special Issue on Computer Arithmetic), October 1991.

P.Dubey and M.Flynn.
``Branch Strategies: Modeling and Optimization,"
IEEE Transactions on Computers 40(10): 1159--1167. October 1991.

F. F. Lee, M. J. Flynn, and M. Morf.
``High-Performance Multiprocessor Architecture for a 3-D Lattice Gas Model," Third Annual NASA Symposium on VLSI Design, October 1991.

B.Bray and M.J. Flynn.
``Strategies for Branch Target Buffers,"
Proceedings of the 24th Annual International Symposium on Microarchitecture, pages 42--50, Nov 1991.

P. Dubey and G. Adams and M. J. Flynn.
``Spectrum of Choices: Superpipelined, Superscalar, or Multiprocessor?"
Proceedings of the 3rd IEEE Symposium on Parallel and Distributed Processing, pp. 233--240, December 1991.

K. Richardson and M. J. Flynn
"TIME: Tools for Input/ Output and Memory Evaluation"
Proceedings of 25th HICSS, Kauai, Hawaii, pp. 58-66, Vol. 1, January 1992

D. Wong, G. De Micheli, and M. J. Flynn.
``A Bipolar Chip Using Wave Pipelining to Achieve 2.5x Normal Clock Frequency;"
Proceedings, International Solid-State Circuits Conference, pp. 56--57, San Francisco, CA, February 1992.

D. Wong, G. De Micheli, and M. J. Flynn.
``A Bipolar Population Counter Using Wave Pipeliing to Achieve 2.5x Normal Clock Frequency,"
Journal of Solid-State Circuits, May 1992 (more complete version of previous).

D. Wong and M. Flynn.
``Fast Division Using Accurate Quotient Approximations to Reduce the Number of Iterations,"
IEEE Transactions on Computers, August 1992.

J. Mulder and M. Flynn.
"Processor Architecture and Data Buffering".
IEEE Transactions on Computers, Volume 41, Number 10, pages 1211--1222, October 1992.

E. Schwarz and M. j. Flynn.
"Approximating the Sine Function with Combinational Logic."
26th Proceedings of Asilomar Conference on Signals, Systems and Computers} Asilomar, CA October 1992.

N. Quach and M. J. Flynn.
``High-Speed Addition in CMOS."
IEEE Transactions on Computers, 41(12), December 1992.

B. K. Bray and M. J. Flynn.
``Translation Hint Buffers to Reduce Access Time of Physically-Addressed Instruction Caches,"
Micro-25 Conference Proceedings, pages 206-209, December 1992.

W.L. Lynch, B.K. Bray, and M.J. Flynn.
"The effect of page allocation on caches".
Micro-25 Conference Proceedings, pages 222-225, December 1992.

D. Wong, G. De Micheli, and M. J. Flynn.
``Algorithms for Designing High-Performance Digital Circuits Using Wave Pipelining."
IEEE Transactions on CAD/ICAS, 12(1):25-46, January 1993.

K. J. Richardson and M. J. Flynn.
"Strategies to improve I/O cache performance".
Proceedings of the 26th Hawaii International Conference on System Sciences, January 1993.

M. Thapar and B. Delagi and M. J. Flynn.
``Linked List Cache Coherence for Scalable Shared Memory Multiprocessors."
Proceedings of the 7th International Parallel Processing Symposium, April 1993.

F. Klass, M. J. Flynn, and A. J. van de Goor.
``Pushing The Limits of CMOS Technology: A Wave-Pipelined Multiplier."
Proceedings of the Hot Chips Symposium V, Stanford CA, August 1993.

E. M. Schwarz and M. J. Flynn.
``Hardware starting approximation for the square root operation."
Proceedings of the 11th Symposium on Computer Arithmetic, Windsor, Canada, pages 103--111, 1993.

E. Schwarz and M. J. Flynn.
``Parallel High-Radix Non-restoring Division."
Transactions on Computers, 42(10): 1234--1246, October 1993.

D. B. Glasco, B. A. Delagi and M. J. Flynn.
``Update-Based Cache Coherence Protocols for Scalable Shared-Memory Multiprocessors."
Proceedings of the 27th Hawaii International Conference on System Sciences, vol. I, pages 534--545, January 1994.

P. Dubey and A. Krishna and M. J. Flynn.
``Analytical Modeling of Multithreaded Pipeline Performance."
Proceedings of the 27th Hawaii International Conference on System Sciences, January 1994.

P. Dubey and G. B. Adams III and M. J. Flynn.
``Evaluating Performance Tradeoffs Between Fine-Grained and Coarse-Grained Alternatives."
IEEE Transactions on Parallel and Distributed Systems 6(1):17--27, January 1994.

G. Byrd, B. Delagi and M. J. Flynn.
``Communication Mechanisms in Shared Memory Multiprocessors."
Proceedings of the International Workshop on Support for Large-Scale Shared Memory Multiprocessors, April 1994.

P. Dubey and M. J. Flynn.
Instruction window size tradeoffs and characterization of program parallelism.
IEEE Transactions on Computers, 43(4):431--442, April 1994.

F. Klass, M. J. Flynn, and A. J. van de Goor.
``A 16X16-bit Static CMOS Wave-Pipelined Multiplier,"
International Symposium on Circuits and Systems, London, May 1994.

D. Wong, F. Klass, K. Nowka, G. De Michelli, and M. J. Flynn.
``Wave Pipelining: From Theory to Practice,"
International Symposium on Circuits and Systems, London, May 1994.

F. Klass, M. J. Flynn, and A. J. van de Goor.
``Fast Multiplication in VLSI Using Wave Pipelining,"
Journal of VLSI Signal Processing, 7(3):233--248, May 1994

D. Glasco, B. Delagi and M. Flynn.
``The Impact of Cache Coherence Protocols on Systems Using Fine-Grain Data Synchronization."
Proceedings of the International Conference on Parallel Architectures and Compilation Techniques.
Montreal, August 1994.

D. Glasco, B. Delagi, and M. Flynn.
``Write Grouping for Update-Based Cache Coherence Protocols."
6th IEEE Symposium on Parallel and Distributed Processing, pages 334-341, October 1994.

P. Dubey and M. Flynn.
``A Bubble Propagation Model for Pipeline Performance."
Journal of Parallel and Distributed Computing, 23(3):330--337, December 1994.

P. Dubey and G. B. Adams III and M. Flynn.
``Evaluating Performance Tradeoffs Between Fine-Grained and Coarse-Grained Alternatives."
IEEE Transactions on Parallel and Distributed Systems, 6(1):17--27, January 1995.

K. Richardson and M. J. Flynn.
``I/O Component Characterization for I/O Cache Designs."
Proceedings of the 3rd Annual Workshop on I/O in Parallel and Distributed Systems (IOPADS), Santa Barbara, April 1995.

M. J. Flynn and K. Nowka and G. Bewick and E. Schwatz and N. Quach.
``The SNAP Project: Towards Sub-Nanosecond Arithmetic."
Proceedings of the 12th Symposium on Computer Arithmetic, Bath, England, pages 75--82, July 1995.

S. F. Oberman and M. J. Flynn.
``Implementing Division and Other Floating-Point Operations: A System Perspective."
Proceedings of SCAN-95, IMACS/GAMM International Symposium
on Scientific Computing, Computer Arithmetic and Validated Numerics. Wuppertal, Germany, pp 103-105.
September 1995.

S. F. Oberman and M. J. Flynn.
``Reducing Division Latency with Reciprocal Caches."
Proceedings of SCAN-95, IMACS/GAMM International Symposium on Scientific Computing, Computer Arithmetic and Validated Numerics.Wuppertal, Germany, pages 106-107. September 1995.

M. J. Flynn.
``The Role of Representation in Computer Architecture."
Proceedings of the Conference on Massively Parallel Processing with Optical Interconnections,
San Antonio, Texas, October 1995.

D. F. Zucker, M. J. Flynn, and Ruby B. Lee.
Improving Performance for Software MPEG Players.
Proceedings of COMPCON 96, Santa Clara, CA, February 1996.

S. Fu and M. J. Flynn.
Optimal On-chip Cache Hierarchy Synthesis with Scaling of Technology.
Proceedings of 15th Annual IEEE International Phoenix Conference on Computer and Communications p.129-35 (IPCCC'96). Phoenix, March 1996
Best Paper Award for IPCCC'96.

M. J. Flynn and K. Rudd.
``Parallel Architectures."
Invited paper. ACM Computer Surveys, special issue celebrating the 50th anniversary of Electronic Computing, 29(1):67--70. March 1996.

S. F. Oberman and M. J. Flynn.
``Reducing Division Latency with Reciprocal Caches."
Reliable Computing, 2(2):147--153, April 1996.

M. J. Flynn, S. Oberman, S. Fu, H. Al-Twaijry, K. Nowka, G. Bewick, E. Schwarz, and N. Quach.
``The SNAP Project: Towards Sub-Nanosecond Arithmetic."
Proceedings of the NSF/MIPS Conference on Experimental Research on Computer Systems, June 1996.

D. F. Zucker, M. J. Flynn, and Ruby B. Lee.
``A Comparison of Hardware Prefetching Techniques for Multimedia Benchmarks."
Proceedings of International Conference on Multimedia Computing and Systems 236-44. Hiroshima, Japan, June 1996.

S. F. Oberman and M. J. Flynn.
``A Variable Latency Pipelined Floating-Point Adder."
Proceedings of Euro-Par'96. Lyon, France, Springer LNCS vol. 1124, pp. 183--192, August 1996.

S. T. Fu, D. F. Zucker, and M. J. Flynn.
``Memory Hierarchy Synthesis of a Multimedia Embedded Processor."
Proceedings of ICCD, pp.176—184, October 1996.

P. K. Dubey and M. J. Flynn.
"Optimal Pipelining (and) Branch Strategies", reprinted.
Performance Modeling for Computer Architects, C. M. Krishna, editor. IEEE Computer Society Press, 1996.

S. Oberman and M. J. Flynn.
"Implementing Division and Other Floating-Point Operations: A System Perspective".
Chapter in G. Alefeld and A. Frommer, Ed. Scientific Computing and Validated Numerics, Mathematical Research series, pp.18--24. Akademie Verlag, 1996.

M. J. Flynn.
Foreword to A. Zomaya, Ed. Parallel and Distributed Computing Handbook
McGraw Hill, July 1996.

M. J. Flynn.
Foreword to V. Milutinovic, Surviving the Design of a 200 MHz RISC Processor: Lessons Learned.
IEEE Computer Society Press, November 1996.

M. J. Flynn.
``Parallel processors were the future and they yet may be."
Invited paper, Computer, 29(7):151--152, December 1996.

E. Schwarz and M. J. Flynn.
"Hardware Starting Approximation Method and its Application to the Square Root Operation."
IEEE Transactions on Computers 45(12):1356-1369. December 1996.

M. J. Flynn and K. Rudd.
``Parallel Architectures" chapter
In Handbook of Computer Science and Engineering. Allan Tucker, editor. CRC Press, 1996.

D. F. Zucker, R. B. Lee, and M. J. Flynn.
``Achieving Subword Parallelism by Software Reuse of the Floating Point Data Path."
Multimedia Hardware Architectures, vol. 30(21):51-64, February 1997.

S. Oberman and M. J. Flynn.
``Design Issues in Division and Other Floating-Point Operations."
IEEE Transactions on Computers, 46(2): 154--161, February 1997.

A. Yu, R. Lee, and M. J. Flynn.
``An evaluation of video fidelity metrics."
COMPCON Spring 97, 42nd IEEE Computer Society International Conference Proceedings, p. 49-55. February 1997.

M. J. Flynn.
``Introduction to
`Influence of Programming Techniques on the Design of Computers'."
Proceedings of the IEEE 85(3): 467--469, March 1997.

K. Rudd and M. J. Flynn.
Instruction-Level Parallel Processors-Dynamic and Static Scheduling Tradeoffs.
Proceedings of pAs'97, Aizu, Japan, March 1997.

S. T. Fu and M. J. Flynn.
"Memory Hierarchy Synthesis"
Journal of Simulation, Invited paper, May 1997.

G. T. Byrd and M. J. Flynn.
``Evaluation of Communication Mechanisms in Invalidate-Based Shared Memory Multiprocessors."
Parallel Computer Routing and Communication Workshop, June 1997.

S. F. Oberman, H. Al-Twaijry, and M. J. Flynn.
``The SNAP Project: Design of Floating Point Arithmetic Units."
Proceedings of the 13th IEEE Symposium on Computer Arithmetic, July 1997.

S. Oberman and M. J. Flynn.
``Division Algorithms and Implementations."
IEEE Transactions on Computers, 46(8):833--854, August 1997.

S. F. Oberman, H. Al-Twaijry, and M. J. Flynn.
Invited paper.``Advances in High Performance Floating point Unit Design."
Proceedings of IMACS'97, Berlin, August 1997.

M. J. Flynn.
``What's Ahead in Computer Design?"
Invited keynote, Euromicro'97 Proceedings, Budapest, pages 4--9, September 1997.

M. J. Flynn. Invited keynote.
``Time and Area Optimization in Processor Architecture."
Proceedings of ARCS'97, pp.1--9, Rostock, Germany, September 1997.

A. Yu, R. Lee, and M. J. Flynn.
``Early Detection of All-Zero Coefficients in H.263,"
Picture Coding Symposium Proceedings}, Berlin, September 1997.

H. A. Al-Twaijry, S. F. Oberman, S. T. Fu and M. J. Flynn.
``The SNAP Project: Building Validated Floating Point Units."
Proceedings of SCAN`97} Lyons, September 1997.

A. Yu, R. Lee, and M. J. Flynn.
``Performance enhancement of H.263 encoder based on zero coefficient prediction."
Proceedings of the Fifth ACM International Multimedia Conference}, p. 21-29, November, 1997.

J. Bennett and M. J. Flynn.
``Prediction Caches for Superscalar Processors."
Proceedings of Micro-30, December 1997.

M. J. Flynn.
Foreword to K. Hwang and Z. Xu: Scalable Parallel Computing. McGraw Hill, 1998.

D. F. Zucker, R. B. Lee, and M. J. Flynn.
``An Automated Method for Software Controlled Cache Prefetching."
Proceedings of the 31st Hawaii International Conference on System Sciences, vol.7 p.106-114 Kona, Hawaii, January 1998.

G. T. Byrd and M. J. Flynn.
``Effectiveness of Producer-Initiated Communication."
Proceedings of Hawaii International Conference on System Sciences, January 1998.

S. F. Oberman and M. J. Flynn.
``Minimizing the Complexity of SRT Tables."
IEEE Transactions on VLSI Systems, 6(1):141--149, March 1998.

S. F. Oberman and M. J. Flynn.
``Reducing the Mean Latency of Floating Point Addition."
Theoretical Computer Science, 196(1): 201--214, April 1998.

M. J. Flynn.
``Some Reflections on Computer Engineering:30 Years after the 360 Model 91."
IEEE Computer, April 1998, (Also Keynote talk, Micro-30, Durham NC, December 1997).

O. Mencer, M. Morf, M. J. Flynn.
``PAM-Blox: High Performance FPGA Design for Adaptive Computing."
Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, Napa Valley, April 1998.

O. Mencer, M. Morf, M. J. Flynn.
``Programmability, Performance and Power of FPGA based Computing Machines."
DARPA PI Adaptive Computing Systems Meeting, Napa, April 1998.

O. Mencer, M. Morf, M. J. Flynn.
``Hardware Software Tri-Design of Encryption for Mobile Communication Units."
IEEE International Conference on Acoustics, Speech and Signal Processing, Seattle, May 1998.

O. Mencer, M. Morf, M. J. Flynn.
``Pipelined CORDICs for Reconfigurable Computing."
Proceedings of the Sixth FPGA/PLD Design Conference, Yokohama, Japan, June 1998.

H. Al-Twaijry and M. J. Flynn.
``Technology Scaling Effects on Multipliers."
IEEE Transactions on Computers, 47(11):1201--1215, November 1998.

A. Yu and M. J. Flynn,
“Implementation and Optimization Issues for the H.263 Compression Standard”
Proceedings 32nd Asilomar Conference on Signals, Systems, and Computers, November 1998.

O. Mencer, M. Shand, M. J. Flynn,
“FireLink: A High-Performance Adaptive Firewire Interface”,
IEEE Computer, special issue on High Performance Network Interfaces, Fall 1998.
(Also DEC Digital Systems Research Center TechNote 1998-012.)

G. Byrd and M. J. Flynn.
``CC-NUMA Communication Mechanisms."
ONR N00014-93-1-1335

M. J. Flynn.
``Basic Issues in Microprocessor Architecture."
Journal of System Architecture, 45, 939--948. (Special issue on microprocessor architecture), January 1998.

G. Byrd and M. J. Flynn.
`Producer--Consumer Communication in Distributed Shared Memory Multiprocessors."
Proceedings of the IEEE, 87(3):456-466, March 1999.

D. Sunada, D. Glasco and M. J. Flynn.
"Novel Checkpointing Algorithm for Fault Tolerance".
Proceedings of the 29th International Symposium on Fault-Tolerant Computing, Madison, WI., June 1999.

O. Mencer, M. Morf, M. J. Flynn,
"Precision of Semi-Exact Redundant Continued Fraction Arithmetic for VLSI",
SPIE '99 (Arithmetic session), Denver. July 1999.

M. J. Flynn, P. Hung and K. Rudd,
"Deep-Submicron microprocessor design issues".
IEEE Micro, 19(4):11--22, July/Aug. 1999.

P. Hung, H. Fahmy, O. Mencer and M. J. Flynn,
"Fast Division Algorithms with a Small Lookup Table".
Proceedings of the 33rd Asilomar Conference on Signals, Systems, and Computers, November 1999.

O. Mencer, A. Liddicoat and M. J. Flynn.
"Efficient Digit – Serial Rational Function Evaluation and Digital Filtering Applications".
Proceedings of the 33rd Asilomar Conference on Signals, Systems, and Computers, November 1999.

P. Hung and M. J. Flynn.
"Deep Sub-Micron VLSI Floorplanning Algorithm".
Proceedings of the Electronic Devices and Systems Conference, p 84-87, December 1999.

H. -Y. Lee and M. J. Flynn.
"High-Speed Interconnect Schemes for a Pipelined FPGA".
IEE Proceedings; Computers and Digital Techniques, Special issue on Reconfigurable Systems, 147(3): 195-202. May 2000.

P. Hung and M. J. Flynn.
"Designing Future Microprocessors".
Proceeds of the First International Conference on Parallel and Distributed Computing, Applications and Technologies: PDCAT2000} Hong Kong, May 2000.

H.-Y. Lee, A. Liddicoat and M. J. Flynn.
"Exploiting Parallelism and Data Locality of Systolic Arrays using a Multi – ported FPGA".
International Conference on Parallel and Distributed Processing Techniques and Applications} Vol 1 229-235, Las Vegas, June 2000

A. Liddicoat and M. .J. Flynn.
"Reciprocal Approximation Theory with Table Compression".
SPIE Annual Conference, July 2000.

M. J. Flynn, P. Hung and A. Peymandoust.
"Using Simple Tools to Evaluate Complex Architectural Tradeoffs".
IEEE Micro, 20(4) 2-10, July/August 2000.

D. Zucker, R. B. Lee, M. J. Flynn.
"Hardware and Software Cache Prefetching Techniques for MGEG Benchmarks".
IEEE Transactions on Circuits and Systems for Video Technology, 10(5) 782-796, August 2000

O. Mencer. H. Hubert, P. Hung, M. Morf, M. J. Flynn.
"StReAm: Object-Oriented Programming of Stream Architectures using PAM-Blox".
Proceedings of the PACT 2000 Symposium, Villach, Austria, August 2000

A. Liddicoat and M. J. Flynn.
"Parallel Square and Cube Computation".
Proceedings of the 34rd Asilomar Conference on Signals, Systems, and Computers, October 2000.

M. J. Flynn
"Microprogramming" (and other articles)
Encyclopedia of Computer Science, 4th Edition, Editors A. Ralston et al, Nature Publishing Group, London, 2000.

(A note on the above citation). The Encyclopedia was reissued by J. Wiley and Sons Ltd, West Sussex, UK in 2003.

O. Mencer, M. Platzner, M. Morf and M. J. Flynn.
"Object-oriented Domain-specific Compilers for Programming FPGAs"
IEEE Transactions on VLSI, special issue on Reconfigurable Computing. Feb 2001.

A. Liddicoat and M. J. Flynn
"VLSI and Algorithms for High-Speed Arithmetic"
COOL Chips IV Conference Proceedings, Tokyo, Japan, April 2001

M. J. Flynn and P. Hung
"Computer Architecture"
In Electronic and Electrical Engineering Encyclopedia, pub, J. Wiley, 2001.

M. J. Flynn and A. Liddicoat
"Technology Trends and Adaptive Computing"
Proceedings of FPL 2001, Belfast N. Ireland, August 2001 p 1-5; (an invited keynote lecture/paper)
Lecture Notes in Computer Science, 2147 Springer 2001, ISBN 3-540-42499-7

Albert A. Liddicoat and Michael J. Flynn
"High-Performance Floating Point Divide"
Euromicro Symposium on Digital System Design pages 354-361, Warsaw, Poland, September 2001

Hossam Fahmy, Albert Liddicoat and Michael J. Flynn
"Improving the Effectiveness of Floating Point Arithmetic,"
Proceedings of the 35th Asilomar Conference on Signals, Systems, and Computers, November 2001.

Clecio D. Lima, Kentaro Sano, Hiroaki Kobayashi, Tadao Nakamura and Michael J. Flynn
"A Technology-Scalable Multithreaded Architecture"
Proceedings of SBAC 2001(13th Symposium of Computer Architecture), Sao Paulo, Brazil, September 2001

M. J. Flynn and P. Hung
"CAD Tools for System-Level Modeling and Implementation"
Software Focus (pub. By J. Wiley), Vol. 2, No. 4, December 2001

M. J. Flynn.
Foreword to V. Milutinovic, *Surviving the Design of Infrastructure for Electronic Business on the Internet: Lessons Learned*. Pub. Kluwer Academic, 2001.

Hossam A.H. Fahmy, Albert A. Liddicoat and Michael J. Flynn.
"Parametric Time delay modeling for floating point units"
The International Symposium on Optical Science and Technology, SPIE's 47th annual meeting (Arithmetic session), Seattle, Washington USA, July 2002.

M. J. Flynn
"Programmed Solutions: the step beyond Programmed Logic"
Proceedings of ICFPL, Hong Kong, December 2002

Hossam A.H. Fahmy and M. J. Flynn.
"A case for a Redundant Format in Floating Point Arithmetic"
Proceedings of the 16th IEEE Symposium on Computer Arithmetic Santiago de Compostela, Spain, June 2003

Hossam A.H. Fahmy and M. J. Flynn.
"Rounding in a redundant digit floating point system"
The International Symposium on Optical Science and Technology, SPIE's 48th annual meeting (Arithmetic session), San Diego, CA, August, 2003 (SPIE Vol. 5205)

N. Quach, N. Takagi and M. J. Flynn
"A Systematic IEEE Rounding Method for High-Speed Floating-Point Multipliers"
IEEE Transactions on VLSI Systems, Vol. 12, No. 5, pages 511-521, May 2004

Hossam A.H. Fahmy and M. J. Flynn
"An adder for a redundant digit arithmetic unit".
Proceedings of COOL Chips VII, Yokohama, Japan, April 2004.

M. J. Flynn and P. Dubey
"Introduction to Hot Chips 15" (as guest editors)
IEEE Micro, Vol. 24, No. 2, March- April 2004

M. J. Flynn and P. Hung
"Computer Architecture and Technology: some thoughts on the road ahead"
(Keynote lecture) World Academy of Science Multi Conference of Computer Science and Engineering,
Proceedings of International Conference on Engineering of Reconfigurable Systems and Algorithms 2004, (ERSA'04), pages 3-13, Las Vegas, NV, June 21 2004

S. T. Fu and M. J. Flynn
"FUPA: Floating Point Unit Cost- Performance Metric and its applications to Microprocessors"
IEEE Transactions on VLSI Systems, to appear.

M. J. Flynn and P. Hung
"Microprocessor design issues: some thoughts on the road ahead"
IEEE Micro, to appear March-April 2005

Oskar Mencer, Jacob A. Bower, Wayne Luk, Michael J. Flynn, Martin Morf
"Dynamically Calibrating Clock-Rate for FPGAs"
Proceedings of COOL Chips VIII, Yokohama, Japan, April 2005.

Publications II: Technical Reports

NOTE: CSL-TR in the following refers to the Stanford University's Computer System Lab. technical reports.

M. J. Flynn.
``Complementary Transistor Resistor Latch."
IBM Technical Disclosure Bulletin, 1(6):20, IBM Poughkeepsie, N. Y., April 1959.

M. J. Flynn.
``Complementary Transistor Resistor Adder."
IBM Technical Disclosure Bulletin, 1(6):21, IBM Poughkeepsie, N. Y ,April 1959.

M. J. Flynn. ``Change Adder."
IBM Technical Disclosure Bulletin, 1(6):22, IBM Poughkeepsie, N. Y ,April 1959.

M. J. Flynn. ``Change Control Amplifiers."
IBM Technical Publication, IBM Poughkeepsie, N. Y, 1959.

M. J. Flynn and Robert E. Machol.
``Logical and Functional Specification of Associative Memory."
IBM Technical Report TR.00.852, IBM Poughkeepsie, N. Y , 15 February 1962.

M. J. Flynn and D. S. Henderson.
``Variable Field-Length Data Manipulation."
IBM Technical Report TR.00.862, IBM Poughkeepsie, N. Y, 2 April 1962.

M. J. Flynn.
``Large, High Speed Computer Design: Technology."
IBM Technical Report TR.00.1226, IBM Poughkeepsie, N. Y, 18 December 1964.

M. J. Flynn.
Shared Internal Resources in a Multiprocessor.
Johns Hopkins University Computer Research Report #2 NYO-4209-2., April 1971.

R. W. Cook and M. J. Flynn.
Entropy Functions in a Metric Space.
Johns Hopkins University Computer Research Report #4 NYO-4209-4, April 1971.

R. W. Cook and M. J. Flynn.
Time and Space Measures of Finite Functions.
Johns Hopkins University Computer Research Report #5 NYO-4209-5, December 1971.

G. Tjaden and M. J. Flynn.
Representation of Concurrency Matricies.
Johns Hopkins University Computer Research Report #23 CHO-3288-23, October 1972.

M. J. Flynn.
Studies in the Organization of Computer Systems.
Johns Hopkins University Report #34.
(Final Report for Atomic Energy Commission #AT(11-1)-3288, 6/15/70--12/31/74).

M. J. Flynn, L. Hoevel and C. Neuhauser.
The Stanford Emulation Laboratory.
CSL-TR-118.

M. J. Flynn and L. Hoevel.
Interpretive Architectures: A Theory of Ideal Language Machines.
CSL-TR-79-170, February 1979.

L. Hoevel and M. J. Flynn.
A Theory of Interpretive Architectures: Some Notes on DEL Design and a FORTRAN Case Study.
CSL-TR-79-171, February 1979.

S. F. Lundstrom and M. J. Flynn.
Design of Testbed and Emulation Tools.
CSL-TR-86-309, September 1986.

M. J. Flynn and S. Lundstrom.
Design of Testbed and Emulation Tools.
CSL-TR-88-337, November 1988.

M. J. Flynn, P. Kanerva and N. Bhadkamkar
Sparse, Distributed Memory Prototype: Principles of Operation.
CSL-TR-88-338, December 1988.

M. J. Flynn, R. Zeidman and E. Lochner.
Sparse Distributed Memory Prototype: Address Module Hardware Guide.
CSL-TR-88-373, December 1988.

K. J. Cuderman and M. J. Flynn.
The Relative Effects of Optimization on Instruction Architecture Performance.
CSL-TR-89-398, October 1989.

D. Wong, G. De Micheli, and M. Flynn.
Inserting Active Delay Elements to Achieve Wave Pipelining.
CSL-TR-89-386, November 1989.

M. J. Flynn, P. Kanerva and N. Bhadkamkar.
Sparse Distributed Memory: Principles and Operation.
CSL-TR-89-400, November 1989.

P. K. Dubey and M. J. Flynn.
Branch Strategies: Modeling and Optimization.
CSL-TR-90-411, February 1990.

J. M. Mulder, N. T. Quach and M. J. Flynn.
An Area-Utility Model for On-Chip Memories and its Application.
CSL-TR-90-413, February 1990.

N. T. Quach and M. J. Flynn.
High-Speed Addition in CMOS.
CSL-TR-90-415, February 1990.

F. F. Lee, M. J. Flynn, and M. Morf.
A VLSI Architecture for the FCHC Isometric Lattice Gas Model.
CSL-TR-90-426, April 1990.

M. J. Flynn, Giovanni De,Micheli, Robert Dutton, Bruce Wooley, and Fabian Pease.
Sub-Nanosecond Arithmetic.
CSL-TR-90-428, May 1990.

N. Quach and M. J. Flynn.
An Improved Algorithm for High-Speed Floating Point Addition.
CSL-TR-90-442, August 1990.

M. Ogata and M. J. Flynn.
A Queuing Analysis for Disk Array Systems.
CSL-TR-90-443, August 1990.

B. K. Bray, W. L. Lynch, and M. J. Flynn.
Page Allocation to Reduce Access Time of Physical Caches.
CSL-TR-90-454, November 1990.

M. J. Flynn.
Research in Concurrent Systems.
CSL-TR-90-455, December 1990.

N. T. Quach, N. Takagi, and M. J. Flynn.
On Fast IEEE Rounding.
CSL-TR-91-459, January 1991.

N. T. Quach and M. J. Flynn.
Leading One Prediction---Implementation, Generalization, and Application.
CSL-TR-91-463, March 1991.

B. K. Bray and M. J. Flynn.
Write Caches as an Alternative to Write Buffers.
CSL-TR-91-470, April 1991.

M. J. Flynn and B. K. Bray.
Strategies For Branch Target Buffers.
CSL-TR-91-480, June 1991.

P. Dubey and G. Adams and M. Flynn.
Exploiting Fine-Grain Concurrency: Analytical Insights in Superscalar Processor Design.
Purdue Technical Report TR-EE 91-31, August 1991.

M. J. Flynn.
Subnanosecond Arithmetic (Second Report).
CSL-TR-91-481, June 1991.

N. Quach and M. J. Flynn.
Suggestions for Implementing a Fast IEEE Multiply-Add-Fused Instruction.
CSL-TR-91-483, July 1991.

W. L. Lynch and M. J. Flynn.
Paging Performance with Page Coloring.
CSL-TR-91-492, October 1991.

B. K. Bray and M. J. Flynn.
A Two-Level Windowed Register File.
CSL-TR-91-499, December 1991.

N. Quach and M. J. Flynn.
Design and Implementation of the SNAP Floating-Point Adder.
CSL-TR-91-501, December 1991.

M. J. Flynn.
Research in Concurrent Systems (Report for 1991).
CSL-TR-92-502, January 1992.

B. K. Bray and M. J. Flynn.
Tag Caching for Improving Write-Back Cache Bandwidth.
CSL-TR-92-509, February 1992.

B. K. Bray and M. J. Flynn.
Efficiently Supporting Subword Loads and Stores.
CSL-TR-92-514, April 1992.

E. M. Schwarz and M. J. Flynn.
Direct Combinational Methods for Approximating Trigonometric Functions.
CSL-TR-92-525, May 1992.

Gary Bewick and M. J. Flynn.
Binary Multiplication Using Partially Redundant Multiples.
CSL-TR-92-528, June 1992

N. Quach and M. J. Flynn.
A Radix-64 Floating-Point Divider.
CSL-TR-92-529, June 1992.

B. Flachs and M. J. Flynn.
Sparse Adaptive Memory.
CSL-TR-92-530, June 1992.

B. K. Bray and M. J. Flynn.
Translation Hint Buffers to Reduce Access Time of Physically-Addressed Instruction Caches.
CSL-TR-92-535, August 1992.

E. M. Schwarz and M. J. Flynn.
Using a Floating-Point Multiplier to Sum Signed Boolean Elements.
CSL-TR-92-540, August 1992.

E. M. Schwarz and M. J. Flynn.
Using a Floating-Point Multiplier's Internals for High-Radix Division and Square Root.
CSL-TR-93-554, January 1993.

B. K. Bray and M. J. Flynn.
Fetch Caches.
CSL-TR-93-561, February 1993.

M. J. Flynn.
Research in Computer Architecture.
CSL-TR-93-571, January 1993.

M. J. Flynn, G. DeMicheli, R. F. Pease, and B. Wooley.
Subnanosecond Arithmetic.
CSL-TR-93-572, May 1993.

F. Klass and M. J. Flynn.
Comparative Studies of Pipelined Circuits.
CSL-TR-93-579, July 1993.

B. Flachs and M. J. Flynn.
Sparse Adaptive Memory: Learning Heuristics.
CSL-TR-93-582, August 1993.

D. B. Glasco, Bruce A. Delagi and M. J. Flynn.
Update-Based Cache Coherence Protocols for Scalable Shared-Memory Multiprocessors.
CSL-TR-93-588, January 1994.

B. Zhang, M. J. Flynn and Fung F. Lee.
Design of General Collision Unit for Three-Dimensional Lattice Gas Models.
CSL-TR-94-598, January 1994.

S. Oberman, Nhon Quach, and M. Flynn.
The Design and Implementation of a High-Performance Floating-Point Divider.
CSL-TR-94-599, January 1994.

K. J. Nowka and M. J. Flynn.
Environmental Limits on the Performance of CMOS Wave-Pipelined Circuits.
CSL-TR-94-600, January 1994.

K. J. Nowka and M. J. Flynn.
Wave Pipelining of High Performance CMOS Static RAM.
CSL-TR-94-615, January 1994.

S. Fu and M. Flynn.
Area and Performance Analysis of Processor Configurations with Scaling of Technology.
CSL-TR-94-605, March 1994.

D. B. Glasco, Bruce A. Delagi, and M. J. Flynn.
The Impact of Cache Coherence Protocols on Systems Using Fine-Grain Data Synchronization.
CSL-TR-94-611, March 1994.

D. B. Glasco, Bruce A. Delagi, and M. J. Flynn.
Write Grouping for Update-Based Cache Coherence Protocols.
CSL-TR-94-612, March 1994.

D. B. Glasco, B. A. Delagi, and M. J. Flynn.
Design and Validation of Update-Based Cache Coherence Protocols.
CSL-TR-94-613, March 1994.

P. Dubey, A. Krishna, and M. Flynn.
Analytical Performance Modeling for a Spectrum of Multithreaded Machines.
IBM Research Report RC 19549, May 1994.

G. Byrd, B. Delagi and M. Flynn.
Communication Mechanisms in Shared Memory Multiprocessors.
CSL-TR-94-623, May 1994.

Osamu Okuzawa and M. J. Flynn.
A Performance/Area Workbench for Cache Memory Design.
CSL-TR-94-635, August 1994.

J. E. Bennett and M. J. Flynn.
Two Case Studies in Latency Tolerant Architectures.
CSL-TR-94-639, October 1994.

S. F. Oberman and M. J. Flynn.
Design Issues in Floating-Point Division.
CSL-TR-94-647, December 1994.

H. Al-Twaijry and M. Flynn.
Multipliers and Datapaths.
CSL-TR-94-654, December 1994.

J. E. Bennett and M. J. Flynn.
Performance Factors for Superscalar Processors.
CSL-TR-95-661, February 1995.

S. F. Oberman and M. J. Flynn.
On Division and Reciprocal Caches.
CSL-TR-95-666, April 1995.

S. Fu, Nhon Quach and M. Flynn.
Architecture Evaluator's Workbench and its Application to Microprocessor Floating Point Units.
CSL-TR-95-668, June 1995.

G. McFarland and M. Flynn.
Delay Models for CMOS Circuits.
CSL-TR-95-672, June 1995.

S. Oberman and M. Flynn.
An Analysis of Division Algorithms and Implementations.
CSL-TR-95-675, July 1995.

G. McFarland and M. Flynn.
Limits of Scaling MOSFETs.
CSL-TR-95-662, November 1995.

S. F. Oberman and M. J. Flynn.
Measuring the Complexity of SRT Tables.
CSL-TR-95-679, November 1995.

H. Al-Twaijry and M. Flynn.
Performance/Area Tradeoffs in Booth Multipliers.
CSL-TR-95-684, November 1995.

D. F. Zucker, M. J. Flynn, and Ruby B. Lee.
A Comparison of Hardware Prefetching Techniques for Multimedia Benchmarks,
CSL-TR-95-683, December 1995.

J. Bennett and M. Flynn.
Latency Tolerance for Dynamic Processors.
CSL-TR-96-687, January 1996.

S. Oberman and M. Flynn.
A Variable Latency Pipelined Floating-Point Adder.
CSL-TR-96-689, February 1996.

H. Kishigami, K. Nowka, and M. Flynn.
Delay Balancing of Wave Pipelined Multiplier Counter Trees
Using Pass Transistor Multiplexers.
CSL-TR-96-692, January 1996.

H. Al-Twaijry and M. Flynn.
Technology Scaling Effects on Multipliers.
CSL-TR-96-698, July 1996.

S. F. Oberman and M. J. Flynn.
Fast IEEE Rounding for Division by Functional Iteration.
CSL-TR-96-700, July 1996.

H. Al-Twaijry and M. J. Flynn.
Optimum Placement and Routing of Multiplier Partial Product Trees.
CSL-TR-96-706, October 1996.

J. E. Bennett and M. J. Flynn.
Reducing Cache Miss Rates Using Prediction Caches.
CSL-TR-96-707, October 1996.

D. Sunada, D. Glasco and M. Flynn.
Fault Tolerance: Methods of Rollback Recovery.
CSL-TR-97-718, March 1997.

H.-J. Lee, M. Morf and M. Flynn.
Packet Switching Photonic Network Switch Design and Routing Algorithm.
CSL-TR-97-734, December 1997.

P. Hung and M. Flynn.
Stochastic Congestion Model for VLSI Systems.
CSL-TR-97-737, October 1997.

O. Mencer and M. Flynn.
Selection of Recent Advances in Computer Architecture.
CSL-TR-97-745, December 1997.

D. Sunada, D. Glasco and M. Flynn.
ABSS v2.0: a SPARC Simulator.
CSL-TR-98-755, April 1998.

D. Sunada, D. Glasco and M. Flynn.
Hardware-assisted Algorithms for Checkpoints.
CSL-TR-98-756, July 1998.

O. Mencer, M. Shand, and M. Flynn.
``FireLink: A High-Performance Adaptive Firewire Interface."

DIGITAL Systems Research Center TechNote 1998-012, June 1998.
(Also in the IEEE Computer special issue on Network Interfaces.)

H.-J. Lee and M. J. Flynn.
Designing a Partitionable Multiplier.
CSL-TR-98-772, October 1998.

D. Sunada, D. Glasco and M. Flynn.
Novel Checkpointing Algorithm for Fault Tolerance
on a Tightly-Coupled Multiprocessor.
CSL-TR-99-776, January 1999.

H.-J. Lee and M. J. Flynn.
Coarse Grain Carry Architecture for FPGA.
CSL-TR-99-780, February 1999.

P. Hung and M. J. Flynn.
Optimum ILP for Superscalar and VLIW Processors.
CSL-TR-99-783, August 1999.

H.-J. Lee and M. J. Flynn.
High Speed Interconnect Schemes for Pipelined FPGA.
CSL-TR-99-786, August 1999.

A. Liddicoat and M. J. Flynn.
Reciprocal Approximation Theory with Table Compensation.
CSL-TR-00-790, January 2000.

O. Mencer, M. Morf and M. J. Flynn.
Precision of Semi-Exact Redundant Continued Fraction Arithmetic.
CSL-TR-00-791, Febuary 2000.

O. Mencer, M. Morf and M. J. Flynn.
Performance of Data Intensive Algorithms on FPGAs in an Object-oriented Programming Enviroment..
CSL-TR-00-792, Febuary 2000.

Albert Liddicoat and Michael J. Flynn
Parallel Computation of the Square and Cube Function
CSL-TR-00-808, August 2000.

Albert Liddicoat and Michael J. Flynn
Pipelineable Division Unit ,
CSL-TR-00-809, September 2000

External lectures, presentations, invited and keynote lectures

``Complementary Transistor-Resistor Logic,"
AIEE Winter General Meeting, New York, New York, January 1959.

``Engineering Aspects of Large High-Speed Computer Design,"
Symposium on Microelectronics and Large Systems, (Office of Naval Research), Washington, D. C., 1964

“Large High-Speed Computer Design,"
Argonne National Laboratory, Argonne, Illinois, March 1965

“Systems Engineering”
National lecturer, Bolt, Beranek and Newman, Cambridge, MA, Lectured in New York, Los Angles, Washington D.C., Boston, Houston, April and May 1966

“Large High-Speed Computer Design,"
Northwestern University, Evanston, Illinois, 11 April 1966

“Large High-Speed Computer Design,"
University of Chicago, Chicago, Illinois, 26 April 1966

``A Prospectus in Integrated Electronics and Computer Architecture,"
AFIPS Conference, Fall Joint Computer Conference, San Francisco, CA, 8 November 1966

“Large High-Speed Computer Design,"
IEEE Chicago Chapter, Chicago, Illinois, 28 October 1967.

“Systems Engineering”
National lecturer, Bolt, Beranek and Newman, Cambridge, MA, Lectured in New York, Los Angles, Washington D.C., Boston, March and May 1967

``Intrinsic Multiprocessing,"
AFIPS Conference Proceedings, Spring Joint Computer Conference, Atlantic City, New Jersey, April 1967.
.
``Microprogramming Revisited."
Association of Computing Machinery National Conference, Washington, D.C., 29 August 1967.

“Large High-Speed Computer Design,"
Brookhaven National Laboratory, Brookhaven, New York, 1 November 1967

“Integrated Electronics and Computer Architecture,"
ISSCC, Philadelphia, Pennsylvania, 15 February 1968

“Systems Engineering”
National lecturer, Bolt, Beranek and Newman, Cambridge, MA, Lectured in New York, Los Angles, Washington D.C., March and May 1968

``The Use of a Technology: Function vs. Memory in LSI,"
Second IEEE Computer Group Conference, Los Angeles, CA, June 1968.

``Addressing Patterns and Memory Handling Algorithms,"
Fall Joint Computer Conference, San Francisco, CA. December 1968.

“ Advances in Computer Architecture”.

ISSCC, Philadelphia, Pennsylvania, 20 February 1969

“ Advances in Computer Architecture”.
Bell Telephone Laboratories, Naperville, Illinois, 11 April 1969

“ Advances in Computer Architecture”.
University of Missouri, Rolla, Missouri, 17 April 1969

“Systems Engineering”
National lecturer, Bolt, Beranek and Newman, Cambridge, MA, Lectured in Washington D. C., Los Angles, Boston and White Sands, New Mexico, March and May 1969

“Division by Functional Iteration”
ARITH1, The first IEEE workshop on Computer Arithmetic, Minneapolis, Minnesota, 16 June 1969

``A Multiple Instruction Stream Processor with Shared Resources,"
ONR Symposium on Parallel Processors, Monterey, CA, 26 June 1969

“Organization of Computing Systems”
Conference on Computer and Program Organization, University of Michigan Engineering Summer Conferences, Ann Arbor, 1969

“Organization of Computing Systems”
Workshop on Numerical Methods and Hardware, Lake Arrowhead, California, 25 September 1969

“Dynamic Microprogramming”
MICRO2, The 2nd Workshop on Microprogramming, Phoenix, Arizona, 13 October 1969

“Organization of Computing Systems”
University of Chicago, Chicago, Illinois, 28 October 1969

“Organization of Computing Systems”
Rutgers University, New Jersey, 12 December 1969

``Multi-planer Self-Restricting Mazes: Some Results and Systems Applications,"
Proceedings of the Third Hawaii International Conference on System Sciences, Honolulu, January 15 1970.

“Organization of Computing Systems”
Illinois Institute of Technology, Chicago, Illinois, 28 January 1970

“Systems Engineering”
National lecturer, Bolt, Beranek and Newman, Cambridge, MA, Lectured in New York, N. Y., Baltimore, Orlando, Florida and Washington D. C., February and April 1970

“Organization of Computing Systems”
George Washington University, March 5 1970

“Organization of Computing Systems”
Johns Hopkins University, Baltimore, Maryland, March 1970

“Organization of Computing Systems”
Stanford University, Stanford, California, 8 April 1970

“Organization of Computing Systems”
Houston Conference on Systems Science, Houston, Texas, 21 April 1970

“Organization of Computing Systems”
Southern Methodist University, Dallas, Texas, 22 April 1970

“Computer and Program Organization”
Summer lecturer, University of Michigan, Ann Arbor, Michigan, June 1970

Opening remarks
MICRO3, Buffalo, New York, 12 October 1970

“Large High-Speed Computer Design,"
ACM National lecturer, Bucknell University, Lewisberg, Pennsylvania, 11 November 1971

“Microprogramming”
ISSCC, Philadelphia, Pennsylvania, 18 February 1971

``Microprogramming: Future Prospects and Trends,"
IEEE International Convention, New York, N. Y., March 23 1971

“Large High-Speed Computer Design,"
ACM National lecturer, University of Missouri, Rolla, Missouri, 14 April 1971

“Large High-Speed Computer Design,"
ACM National lecturer, New Mexico Technical Institute, Sacurro, New Mexico, 15 April 1971

“Large High-Speed Computer Design,"
ACM National lecturer, University of California, Irvine, California, 16 April 1971

``Coding Techniques for Failure Recovery in a Distributive Modular Memory Organization,"
American Federation of Information Processing Societies (AFIPS) Conference (SJCC), Atlantic City, N. J., May 20 1971.

“Large High-Speed Computer Design,"
Manchester University, Manchester, England, May 27 1971

“Computer Engineering”
Summer lecturer, IRIA, Institute de Recherche d'Info. et d'Autom., Paris, June 1971

“Large High-Speed Computer Design,"
University of Paris, Paris, France, June 1971

“Large High-Speed Computer Design,"
Grenoble University, Grenoble, France, June 1971

“Computer Engineering”
Summer lecturer, University of Michigan, Ann Arbor, Michigan, July 1971

``Shared Internal Resources in a Multiprocessor,"
IFIP 71 Congress, Ljubljana, Yugoslavia, August 1971

``Microprogramming: Future Prospects and Trends,"
NATO Workshop on Microprogramming, St. Raphel, France, 1- 7 September 1971

“Large High-Speed Computer Design,"
ACM National lecturer, Chapel Hill, N.C., 2 November 1971

``A Perspective on Computer Reliability,"

1972 Symposium of Reliability and Maintainability, San Francisco, CA, January 1972.

“Large High-Speed Computer Design,"
Harvard University, Cambridge, MA, 24 January 1972

“Large High-Speed Computer Design,"
ACM National lecturer, Annapolis, Maryland, 16 February 1972

“Large High-Speed Computer Design,"
ACM National lecturer, University of Minnesota, Minneapolis, Minnesota, 23 February 1972

“Large High-Speed Computer Design,"
ACM National lecturer, University of Iowa, Iowa City, Iowa, 24 February 1972

“Large High-Speed Computer Design,"
ACM National lecturer, University of Wisconsin- Milwaukee, 25 February 1972

``Multiprocessors with Shared Resources,"
IEEE International Convention, New York, March 1972.

“Microprogramming”
University of Maryland, College Park, Maryland, 12 April 1972

``Toward more efficient computer organizations,"
American Federation of Information Processing Societies (AFIPS) Conference, Spring Joint Computer Conference, Atlantic City, N.J., 18 May 1972

``Pipelining of Arithmetic Functions,"
ARITH2, Workshop on Computer Arithmetic, College Park, Maryland, 15 May 1972.

“Microprogramming”
University of Pennsylvania, Philadelphia, Pennsylvania, 26 June 1972

Microprogramming”
IEEE Baltimore Chapter, Baltimore, Maryland, 14 September 1972

``Pipelining of Arithmetic Functions,"
COMPCON, San Francisco, CA, September 1972.

“Large High-Speed Computer Design,"
Carnagie Mellon University, Pittsburgh, Pennsylvania, 2 October 1972

“Microprogramming”
Westinghouse Electric Corp., Baltimore, Maryland. 16 October 1972

``Open Problems in Microprogamming,"
University of Illinois, Urbana, Illinois, 4 December 1972

Panel Chair
FJCC, Anaheim, California, 5 December 1972

“Advances in Computer Organization”
IEEE-CS Distinguished lecturer, Duke University, Raleigh, North Carolina, 15 December 1973

``Open Problems in Microprogramming,"
Sixth Hawaii International Conference on Systems Sciences, Honolulu, 11 January 1973.

“Advances in Computer Organization”
Control Data Corporation, Minneapolis, Minnesota, 23 January 1973

“Advances in Computer Organization”
Bell Laboratories, Murray Hill, New Jersey, 26 February 1973

“Advances in Computer Organization”
IEEE-CS Distinguished lecturer, Rochester University, Rochester, New York, 27 February1973

“Advances in Computer Organization”
IEEE-CS Distinguished lecturer, Syracuse University, Syracuse, New York, 28 February1973

“Advances in Computer Organization”
Technical University of Berlin, Berlin, Germany, 27 September 1973

“Advances in Computer Organization”
IEEE-CS Distinguished lecturer, Institute for Information Sciences (USC), Los Angles, California, 9 October 1973

“Advances in Computer Organization”
2nd Texas Conference on Computing Systems, Austin, Texas, 13 November 1973

“Advances in Computer Organization”
University of Dortmund, Dortmund, Germany, 6 December 1973

“Advances in Computer Organization”
Stanford University, Stanford, California, 6 March 1974

“Microprogramming”
University of Maryland, College Park, Maryland, 22 March 1974

``Trends and Problems in Computer Organization"
Invited lecture, IFIPS 74 Congress, Stockholm, Sweden, 5 August 1974

Session chair
MICRO 7, Palo Alto, California, October 1974.

“Computer Organizations and their Uses”
3rd Texas Conference on Computer Systems, Austin, Texas, 7 November 1974

“Organization of Computing Systems”
Rice University, Houston, Texas, 8 November 1974

``EMMY: An Emulation System for User Microprogramming,"
National Computer Conference, Anaheim, CA., 22 May 1975.
.
``An Integrated Facility for Emulation Research,'
2nd USA--Japan Computer Conference, Tokyo, Japan, August 1975

Introductory Remarks
ISCA 3, (International Symposium on Computer Architecture), Florida, January 19 1976.

``Non-Specific Computers,"
COMPCON, San Francisco, 24 February 1976.

``Some Remarks on High Speed Computers,"
COMPCON, San Francisco, California, 1 March 1977.

``The Interpretive Interface: Resources and Program Representation in Computer Organization,"
Symposium on High Speed Computers and Algorithm Organization, University of Illinois, Champaign, IL, April 13--15 1977

``Some Remarks on High Speed Computers,"
Technical University of Munich, Munich, Germany, August 1977

``Some Remarks on High Speed Computers,"
CERN, Geneva, Switzerland, August 1977.

``Performance Analysis of Distributed Computer Systems,"
Sixth Texas Conference on Computer Systems}, Austin, Texas, November 1977.

``Non-Specific Computers"
INFOTECH Future Systems Symposium, London, England, 1977.

``Computer Organization and Architecture,"
Lecture series, NATO Workshop on Advanced Operating Systems, Munich, Germany, 27 March- 6 April 1978

``Computer Organization and Architecture,"
Lecture series, NATO Workshop on Advanced Operating Systems, Munich, Germany, 22-26 August 1978

``Some Remarks on High Speed Computers,"
University of Grenoble, Grenoble, France, 22 June 1979

``Parallelism and Representation Problems in Distributed Systems,"
1st International Conference on Distributed Computing Systems, Huntsville, AL, 2 October 1979

``Some Remarks on High Speed Computers,"
University of California, Berkley, California, 25 October 1979

Workshop on Support for High Level Languages, Clearwater, Florida, 27 May 1980

``Computer Organization and Architecture,"
University College Galway, Galway, Ireland, 29 September 1980

“Computer Arithmetic”
University College Galway, Galway, Ireland, 30 October 1980

``Computer Organization and Architecture,"
Queen’s University, Belfast, N. Ireland, 11 March 1981

``Computer Organization and Architecture,"
University of Limerick, Limerick, Ireland, 1981

“Perspective on Microprocessors” and “Customized Microprocessors”
CREST Course (EEC sponsored) on Microprocessor System Design, 29 June- 10 July 1981, Dublin, Ireland

``Analysis of Architectures for High Level Languages,"
Workshop on High-Level Language Computer Architecture, Los Angeles, CA, October 1981

``Computer Organization and Architecture,"
General Electric Research Symposium, Schenectady New York, 16 June 1982

``Computer Organization and Architecture,"
Institute for Management Science, New York, New York, 18 June 1982

``Computer Organization and Architecture,"
Apple Computer Corp., Cupertino, California, 1982

"Evolution of Microprogramming"
Conference Luncheon lecture, MICRO15, Palo Alto, California, 7 October 1982

``Concurrency Detection in Language-Oriented Processing Systems,"
Third International Conference on Distributed Computing Systems, Miami/Ft. Lauderdale, FL, October 1982.

``Performance Evaluation of the Execution Aspects of Computer Architectures,"
International Workshop on High-Level Language Computer Architecture, Ft. Lauderdale, FL, 2 December 1982

``Computer Organization and Architecture,"
Oregon Graduate Center, Portland Oregon, 1 March 1983

``Comparative Analysis of Computer Architectures,"
IFIP Congress '83, Paris, September 1983.

``Directly Executed Language Architectures for VLSI Processor Design,"
IEEE International Conference on Computer Design, New York, NY, October 1983.

``Towards Better Instruction Sets,"
Keynote lecture, MICRO16, Downingtown, Pennsylvania, 12 October 1983

"Tradeoffs in Computer Architecture"
University of California- Berkley, Berkley, California, 26 January 1984

"Tradeoffs in Computer Architecture"
Manchester University, Manchester, England, 3 July 1984

"Tradeoffs in Computer Architecture"
Trinity College, University of Dublin, Dublin, Ireland, 10 July 1984

"Instruction Sets and Microprogramming"
Keynote lecture
MICRO17, Palo Alto, California, 30 October 1984

"Tradeoffs in Computer Architecture"
NASA Ames Research Center, Mountain View, California, 23 July 1985

"Tradeoffs in Computer Architecture"
University of Pittsburgh, Pittsburgh, Pennsylvania, 10 November 1985

"The Stanford Packet Radio Network"
COMPCON Spring '86, San Francisco, California, March 1986

"The Stanford Packet Radio Network"
IBM Science Center, Palo Alto, California, 1 April 1986

“Tradeoffs in Computer Architecture”
Distinguished lecture, University of Southern California, Los Angles, California, 26 September 1986

“The Stanford Packet Radio Network”
IBM Research Center, Yorktown Heights, New York, 17 November 1986

``Mapping between Parallel Processor Structures and Programs,"
20th Hawaii International Conference on Systems Sciences, Honolulu, Hawaii, January 1987

``Effects of Layered Protocols on Performance of a Packet Radio Network,"
COMPCON Spring '87

“Tradeoffs in Processor Architecture”
University of Tokyo, Tokyo, Japan, 24 August 1987

“Tradeoffs in Processor Architecture”
Seoul, Korea, 28 August 1987

“Computer Engineering”
Lecture series, Jaio Tung University, Sponsored by PTT China, Shanghai, China, 31 August- 4 September 1988

“Tradeoffs in Processor Architecture”
Distinguished lecture, Rice University, Houston, Texas, 15 March 1988

“Tradeoffs in Processor Architecture”
Lecture series, Polish Academy of Science, Warsaw, Poland, 27 June- 1 July 1988

“Tradeoffs in Processor Architecture”
University of Texas, Austin, Texas, 23 September 1988

``Approaching a Nanosecond: A 32-bit Adder,"
International Conference on Computer Design, October 1988

“Tradeoffs in Processor Architecture”
Cornell University, Ithaca, New York, 15 December 1988

“Tradeoffs in Processor Architecture”
Computer Forum lecture, Institute for Defense Analysis, Arlington, Virginia, 20 December 1988

CASIS review
Stanford, California, 7 March 1989

“Computer Engineering”
Distinguished lectures, Jaio Tung University, Taiwan, 31 July- 2 August 1989

Opening remarks, also “ASIC Microprocessors”
MICRO22, 22nd International Workshop on Microprogramming, Dublin, Ireland, 14 August 1989

``Designing High-Performance Digital Circuits Using Wave Pipelining,"
IFIP Conference on VLSI, Munich, August 1989.

``The Computer Architect's Workbench," In Proceedings of the IFIP
11th World Computer Congress, San Francisco, August 1989.

``Inserting Active Delay Elements to Achieve Wave Pipelining."
ICCAD '89, pp. 270--273, Santa Clara, CA, November 1989.

``The Pipelined Processor as an Alternative to VLIW,"
Third International Supercomputing Conference, Santa Clara, CA, 1989.

``Parallel Processor Memory Reference Analysis and its Application to Interconnect Architecture,"
5th Distributed Memory Computing Conference, Charleston, SC, April 1990.

"The Architect's Workbench Project"
Computer Forum lecture, Institute for Defense Analysis, Arlington, Virginia, 12 July 1989

"The Architect's Workbench Project"
University of Michigan, Ann Arbor, Michigan, 19 February 1990

"Architectural Performance Analysis and Projections"
Computer Forum lecture, Itoh Techno-Science Co., Tokyo, Japan, 11 July 1990

"The Architect's Workbench Project"
Computer Forum lecture, Matsushita Corp., Osaka, Japan, 17 July 1990

CASIS research review
NASA Headquarters, Washington, D. C., 29 August 1990

"The Architect's Workbench Project"
Purdue University, West Lafayette, Indiana, 30 August 1990

"Instruction Sets and Their Implementations"
Keynote lecture, MICRO23, Orlando, Florida, November 1990

"The Architect's Workbench Project"
Distinguished lecture, UCLA, Los Angles, California, 5 March 1991

"Design of Compact High Performance Processing Elements for the FCHC Lattice Gas Models"
5th SIAM Conference for Scientific Computing, March 1991

"The Architect's Workbench Project"
The DEC Distinguished lecture, Georgia Institute of Technology, Atlanta, Georgia, 7 May 1991

"The Architect's Workbench Project"
Computer Forum lecture, Intel Corp., Santa Clara, California, 4 June 1991

"Fast Division using accurate Quotient Approximations to reduce the number of Iterations"
ARITH10, 10th Symposium on Computer Arithmetic, Grenoble, France, June 1991

"Architectural Mechanisms to Support Three-Dimensional Lattice Gas Simulations"
Third Annual ACM Symposium on Parallel Algorithms and Architectures, July 1991.

``High-Performance Multiprocessor Architecture for a 3-D Lattice Gas Model,"
Third Annual NASA Symposium on VLSI Design, October 1991.

``Strategies for Branch Target Buffers,"
MICRO24, the 24th Annual International Symposium on Micro architecture,
November 1991.

``Spectrum of Choices: Superpipelined, Superscalar, or Multiprocessor?"

3rd IEEE Symposium on Parallel and Distributed Processing, December 1991.

"Instruction Sets and Processor Performance"
Distinguished lecture, Seminar in Computer Architecture, Laboratoire de Systemes Logiques, EPLI, Lausanne, Switzerland, 8 October 1991

"TIME: Tools for Input/ Output and Memory Evaluation"
HICSS, Kauai, Hawaii, 9 January 1992

``A Bipolar Chip Using Wave Pipelining to Achieve 2.5x Normal Clock Frequency;"
ISSCC, International Solid-State Circuits Conference, San Francisco, CA, February 1992.

"Computer Architecture"
Lecture on receipt of the Eckert-Mauchly Award, International Symposium on Computer Architecture, Surfer's Paradise, Queensland, Australia, 20 May 1992

"Arithmetic and the Stanford Nanosecond Arithmetic Processor"
Systems Day on Campus, Stanford University, 11 June 1992

"Representation and Parallelism in Architecture"
Invited lecture, Frontiers 92: Symposium on Massively Parallel Processing, Washington, D.C., 21 October 1992

"Approximating the Sine Function with Combinational Logic."
26th Asilomar Conference on Signals, Systems and Computers, Asilomar, Pacific Grove, CA, October 1992

"Representation and Parallelism in Architecture"
Computer Forum lecture
Supercomputer Research Center, Institute for Defense Analysis, College Park, Maryland, 22 October 1992

``Translation Hint Buffers to Reduce Access Time of Physically-Addressed Instruction Caches,"
MICRO-25, 25th International Conference on Micro architecture/ Microprogramming, December 1992.

"The Effect of Page allocation on Caches"
MICRO-25, 25th International Conference on Micro architecture/ Microprogramming, December 1992

"Trends in Computer Engineering"
Japan, December 1992

"Strategies to improve I/O cache performance".
26th Hawaii International Conference on System Sciences, Kauai, Hawaii, January 1993.

``Linked List Cache Coherence for Scalable Shared Memory Multiprocessors."
7th International Parallel Processing Symposium, April 1993.

"SNAP: towards Sub-nanosecond Arithmetic Processors"
Computer Forum lecture, Institute for Defense Analysis, Alexandria, Virginia, 23 April 1993

"SNAP: towards Sub-nanosecond Arithmetic Processors"
Distinguished lecture, Southern Methodist University, Dallas, Texas, 30 April 1993

``Hardware starting approximation for the square root operation."
ARITH11, 11th Symposium on Computer Arithmetic, Windsor, Canada, June 1993.

``Pushing The Limits of CMOS Technology: A Wave-Pipelined Multiplier."

Proceedings of the Hot Chips Symposium V, Stanford CA, August 1993.

``Update-Based Cache Coherence Protocols for Scalable Shared-Memory Multiprocessors."
27th Hawaii International Conference on System Sciences, Hawaii, January 1994.

``Analytical Modeling of Multithreaded Pipeline Performance."
27th Hawaii International Conference on System Sciences, Hawaii, January 1994.

``Communication Mechanisms in Shared Memory Multiprocessors."
International Workshop on Support for Large-Scale Shared Memory Multiprocessors,
April 1994.

"SNAP: towards Sub-nanosecond Arithmetic Processors"
Tohoku University, Sendai, Japan, 25 April 1994

"SNAP: towards Sub-nanosecond Arithmetic Processors"
Aizu University, Aizu, Japan, 26 April 1994

"SNAP: towards Sub-nanosecond Arithmetic Processors"
Tokyo University, Tokyo, Japan, 27 April 1994

``A 16X16-bit Static CMOS Wave-Pipelined Multiplier,"
International Symposium on Circuits and Systems, London, May 1994.

``Wave Pipelining: From Theory to Practice,"
International Symposium on Circuits and Systems, London, May 1994.

``The Impact of Cache Coherence Protocols on Systems Using Fine-Grain Data Synchronization."
International Conference on Parallel Architectures and Compilation Techniques. Montreal, August 1994.

``Write Grouping for Update-Based Cache Coherence Protocols."
6th IEEE Symposium on Parallel and Distributed Processing, October 1994.

``Wave Pipelining: From Theory to Practice,"
IBM Research, Yorktown Heights, New York, 16 December 1994

``Wave Pipelining: From Theory to Practice,"
University of Belgrade, Belgrade, Yugoslavia FR, 18 April 1995

``I/O Component Characterization for I/O Cache Designs."
3rd Annual Workshop on I/O in Parallel and Distributed Systems (IOPADS)}, Santa Barbara, April 1995.

"Systems Engineering"
Lecture on receipt of the Goode Medal, ICPP 95, Vancouver, British Columbia, Canada, 31 May 1995

"The SNAP Project: Towards Sub-Nanosecond Arithmetic"
ARITH12, 12th Symposium on Computer Arithmetic, Bath, England, 19 July 1995

``Implementing Division and Other Floating-Point Operations: A System Perspective."
SCAN-95, IMACS/GAMM International Symposium on Scientific Computing, Computer Arithmetic and Validated Numerics. Wuppertal, Germany, September 1995.

``Reducing Division Latency with Reciprocal Caches."
SCAN-95, IMACS/GAMM International Symposium on Scientific Computing, Computer Arithmetic and Validated Numerics. Wuppertal, Germany, September 1995.

"The role of Representation in Optimizing a Computer Architecture"
Invited lecture, 2nd International Conference on Massively Parallel Processing using Optical Interconnections (MPPOI 1995), San Antonio, Texas, 23 October 1995

"History of Modern Hardware"
Invited lecture, ACM National conference, on the occasion of the 50th anniversary of the commissioning of the ENIAC, Philadelphia, Pennsylvania, 17 February 1996

"Improving Performance for Software MPEG Players".
COMPCON 96, Santa Clara, CA, February 1996.

"The SNAP Project: Towards Sub-Nanosecond Arithmetic"
GMD Research Institute, Berlin, Germany, 25 March 1996

"Optimal On-chip Cache Hierarchy Synthesis with Scaling of Technology"
15th Annual IEEE International Phoenix Conference on Computer and Communications (IPCCC'96). Phoenix, Arizona, March 1996
Best Paper Award for IPCCC'96.

"The SNAP Project: Towards Sub-Nanosecond Arithmetic"
Distinguished lecture, University of Southern California, Los Angles, 12 April 1996

"The SNAP Project: Towards Sub-Nanosecond Arithmetic"
Kyushu University, Fukuoka, Japan, 22 April 1996

"The SNAP Project: Towards Sub-Nanosecond Arithmetic"
JAIST, Kanazawa, Japan, 24 April 1996

"The SNAP Project: Towards Sub-Nanosecond Arithmetic"
Nagoya University, Nagoya, Japan, 25 April 1996

``The SNAP Project: Towards Sub-Nanosecond Arithmetic."
NSF/MIPS Conference on Experimental Research on Computer Systems, Washington, D.C., June 1996.

``The SNAP Project: Towards Sub-Nanosecond Arithmetic."
Keio University, Tokyo, Japan, 19 June 1996

``The SNAP Project: Towards Sub-Nanosecond Arithmetic."
Tohoku University, Sendai, Japan, 12 June 1996

``A Comparison of Hardware Prefetching Techniques for Multimedia Benchmarks."
International Conference on Multimedia Computing and Systems. Hiroshima, Japan, June 1996.

``A Variable Latency Pipelined Floating-Point Adder."
Euro-Par'96. Lyon, France, August 1996.

"The Stanford Nanosecond Arithmetic Project"
Distinguished lecture, University of Tromso, Tromso, Norway, 16 September 1996

``The SNAP Project: Design of Floating Point Arithmetic Units."
Distinguished lecture, University of Texas, Austin, Texas, 26 September 1996

``Memory Hierarchy Synthesis of a Multimedia Embedded Processor."
ICCD, October 1996

Opening remarks

HPCA 3 (Symposium on High Performance Computer Architecture), San Antonio, Texas, 3 February 1997

``An evaluation of video fidelity metrics."
COMPCON Spring 97, 42nd IEEE Computer Society International Conference, February 1997.

"Instruction-Level Parallel Processors-Dynamic and Static Scheduling Tradeoffs".
pAs'97, Aizu Japan, March 1997.

``The SNAP Project: Design of Floating Point Arithmetic Units."
Osaka University, Osaka, Japan, 23 May 1997

``The SNAP Project: Design of Floating Point Arithmetic Units."
NAIST (Nara Advanced Institute for Science and Technology), Nara, Japan, 26 May 1997

``The SNAP Project: Design of Floating Point Arithmetic Units."
Nagoya University, Nagoya, Japan, 28 May 1997

"Re-configurable Multi-mode, Multi-band Information Transfer System"
DARPA Symposium on Adaptive Computer Systems, Berkley, California, 24 June 1997

``Evaluation of Communication Mechanisms in Invalidate-Based Shared Memory Multiprocessors."
Parallel Computer Routing and Communication Workshop, June 1997.

Opening remarks
ARITH13 (13th Symposium on Computer Arithmetic), Asilomar, Pacific Grove, California, 7 July 1997

``The SNAP Project: Design of Floating Point Arithmetic Units."
ARITH13 (13th Symposium on Computer Arithmetic), Asilomar, Pacific Grove, California, 7 July 1997.

"Advances in High Performance Floating Point Unit Design"
Invited lecture, IMACS1997, Berlin, Germany, 27 August 1997

"What's ahead in Computer Design?"
Keynote lecture, EuroMicro, Budapest, Hungary, 2 September 1997

"Time and area Optimization in processor Architecture"
Keynote lecture, ARCS (Symposium on the Architecture of Computer Systems), Rostock, Germany, 9 September 1997

"What's New in Processor Design?"
San Jose State University, San Jose, California, 9 October 1997

"What's New in Processor Design?"
Computer Forum lecture
Institute for Defense Analysis, Arlington, Virginia, 14 October 1997

"What's New in Processor Design?"
Yonsai University, Seoul, Korea, 27 October 1997

"What's New in Processor Design?"
ETRI (Electro Technology Research Institute), Deaduk, Korea, 29 October 1997

"What's New in Processor Design?"
Chosun University, KwangJu, Korea, 31 October 1997

"Some reflections on Computer Engineering: 30 Years after the 360 Model 91"

Keynote lecture, Micro30, Durham, North Carolina, 2 December 1997

"The SNAP Project: Design of Floating Point Arithmetic Units"
Computer Forum lecture
Intel Corporation, Santa Clara, California, 12 March 1998

``Programmability, Performance and Power of FPGA based Computing Machines."
DARPA PI Adaptive Computing Systems Meeting, Napa, April 1998.

"What's New in Processor Design?"
Sonoma State University, Santa Rosa, California, 7 May 1998

``Hardware Software Tri-Design of Encryption for Mobile Communication Units."
IEEE International Conference on Acoustics, Speech and Signal Processing, Seattle, May 1998.

``Pipelined CORDICs for Reconfigurable Computing."
Sixth FPGA/PLD Design Conference, Yokohama, Japan, June 1998.

"Computer Arithmetic: Past, Present and Future"
University of Belgrade, Belgrade Yugoslavia FR, 27 August, 1998

"Reconfigurable Arithmetic"
Workshop on Multi Media Arithmetic, Saarland, Germany, 1 September 1998

"Re-Configurable Multi-Mode Multi-Band Information Transfer System"
Research review
DARPA Principal Investigators Symposium, Santa Fe, New Mexico, 1 October 1998

"Architectural issues and Nano-Technology"
Photonics and Nano-Technology, Optical Society of America Conference, October 1998

"Computer Arithmetic: Past, Present and Future"
Keynote lecture, FMCAD-98, Palo Alto, California, 4 November 1998

"Reconfigurable Computing and CORDIC Like Architectures"
ICCU'98, Seoul, Korea, November 1998

"Basic Issues in Processor Architecture in the ERA of Deep Submicron Technology"
COOL Chips II, Kyoto, Japan, 27 April, 1999

"Issues in Deep Submicron Microprocessor Architecture"
Nagoya University, Nagoya, Japan, 29 April, 1999

"Basic Issues in Processor Architecture in the ERA of Deep Submicron Technology"
University of Hong Kong, Hong Kong SAR, 18 June 1999

"Basic Issues in Processor Architecture in the ERA of Deep Submicron Technology"
IEEE Workshop on System-on-a-Chip, San Jose, California, 31 July, 1999

"Basic Issues in Processor Architecture in the ERA of Deep Submicron Technology"
Lecture on the occasion of the initiation of the Michael J. Flynn Award for Computer Design
University College Dublin, Dublin, Ireland, 14 October 1999.

"Basic Issues in Processor Architecture in the ERA of Deep Submicron Technology"
Harvey Mudd College, Claremont, California, 13 September 2000

"Basic Issues in Processor Architecture in the ERA of Deep Submicron Technology"
ETH Zurich, Zurich, Switzerland, 19 October 1999

"Issues in Deep Submicron Microprocessor Architecture"
Computer Forum lecture
Institute for Defense Analysis, Arlington, Virginia, 14 January, 2000

"Computer Architecture Beyond the Technology Scaling Era"
Symposium in honor of Professor Edward Davidson, University of Michigan, Ann Arbor, Michigan, 5 May 2000

"Computer Architecture: the Decade Ahead"
Keynote lecture, at ACSAC (Australasian Computer Systems Architecture Conference) and ACSW2001 (Australian Computer Science Week), Bond University, Coolingatta, Queensland, Australia, 29 January 2001.

"Computer Architecture in the Era of Deep Sub Micron Technology"
University of New South Wales, Sydney, Australia, 2 February 2001

"Computer Architecture: the Decade Ahead"
Imperial College, University of London, London, England, 23 May 2001

Keynote lecture, FPL2001 (Symposium of Field Programmable Logic), Belfast, N. Ireland, 25 August 2001

Cheng Tsang Man lectures in Engineering, as Visiting Distinguished Professor, National Technical University (NTU), Singapore, October - November 2001.

Lecture, "Computer Engineering in an era of Sub-Micron technology"
Imperial College, University of London, 1 March 2002

Lecture, "Computer Engineering in an era of Sub-Micron technology"
Queens University, Belfast, NI, 6 March 2002

Lecture, "Computer Engineering in an era of Sub-Micron technology"
Trinity College, University of Dublin, Dublin, 25 March 2002

Special undergraduate lecture, "A computer engineer's tale"
Queens University, Belfast, NI, 10 October 2002

Lecture, "Stanford Nanosecond Arithmetic Processor"
Imperial College, University of London, 17-18 October 2002

Distinguished lecturer, "Computer Engineering in an era of Sub-Micron technology"
SMU, Dallas, TX, 13 November 2002

Keynote lecture, "Programmed Solutions: the step beyond Programmed Logic"
ICFPL 2002, Hong Kong, 17 December 2002

Distinguished lecturer, "Computer Architecture: the road ahead"
University of Texas, Austin, 17 March 2003

Keynote lecture, "Computer Architecture: the road ahead"
ACM Federated Computer Research conferences, San Diego, 10 June 2003

Program Chair's Introduction
Hot Chips 15, Stanford University, Stanford, 18 August 2003

Lecture, "Computer Architecture: the road ahead"
University College, Galway, Ireland, 10 October 2003

Lecture, "Computer Architecture: some thoughts on the road ahead"
Trinity College, University of Dublin, Dublin, 17 October 2003

Lecture, "Computer Architecture: some thoughts on the road ahead"
Delft Technical University, Delft, Netherlands, 20 October 2003

Lecture, "Computer Architecture: some thoughts on the road ahead"
Arithmatica, Warwick, UK, 22 October 2003

Lecture, "Computer Architecture: some thoughts on the road ahead"
Imperial College, University of London, 23 October 2003

Keynote lecture, "Computer Architecture and Technology: the road ahead"
SBAC 2003, Sao Paulo, Brazil, 10 November 2003

Computer Forum Emeritus lecture, "Computer Architecture: the road ahead"
Stanford Univ. 23 February 2004

Keynote lecture, "Computer Architecture: some thoughts on the road ahead"
ERSA conference, Las Vegas, NV, 21 June 2004

Keynote lecture, "Computer Architecture: the road ahead"
IPSI 2004, Pescara, Italy, 29 July 2004

Keynote lecture, "Area-Time-Power tradeoffs in computer design: the road ahead"
High Performance Embedded Computing Conference
MIT Lincoln Laboratories, Lexington MA, 28 September 2004

Lectures (6) on "Custom Computing"
Department of Computing, Imperial College, University of London
January 2005

Keynote lecture,
ASAP 2005 conference
Samos, Greece July 2005